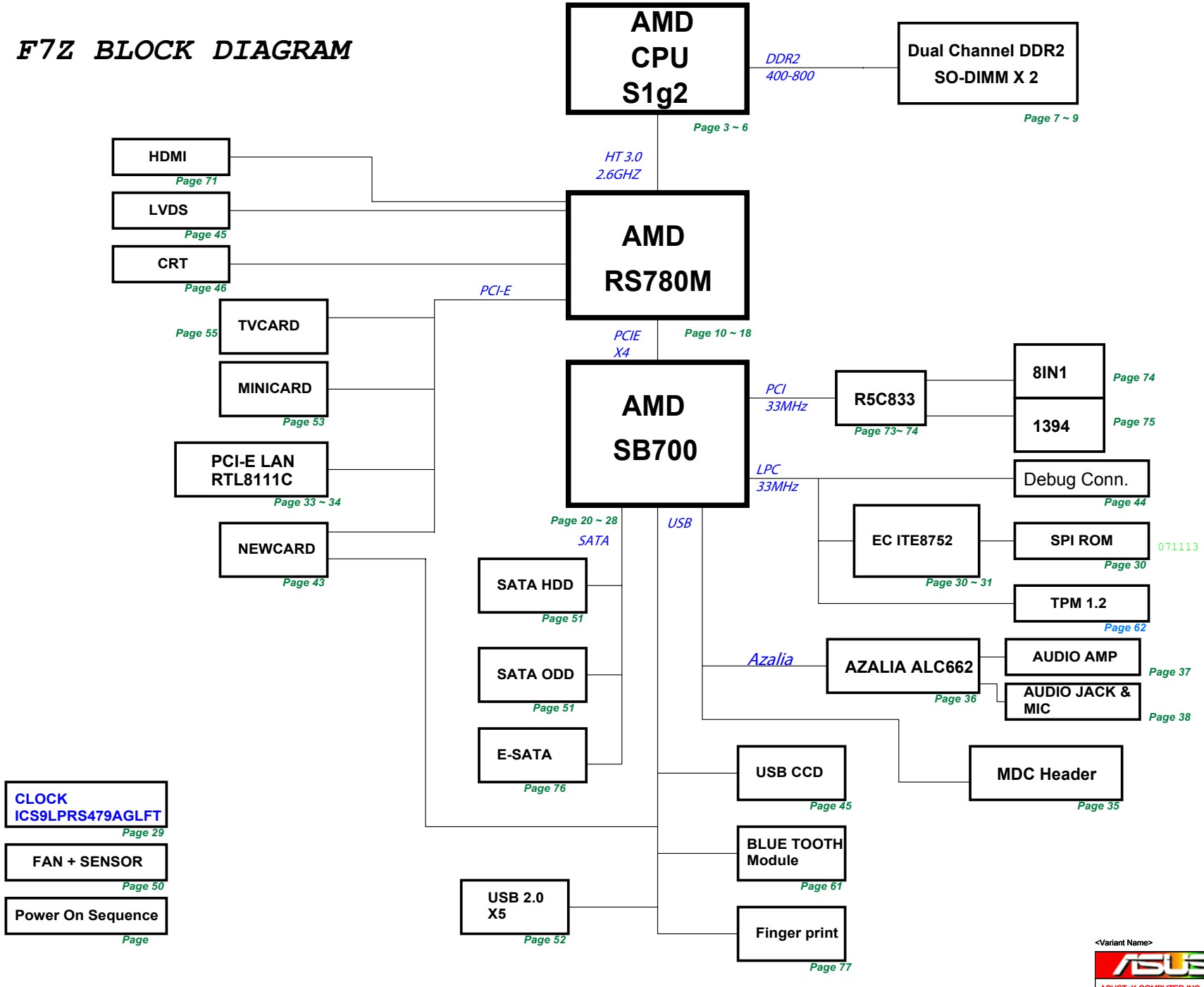
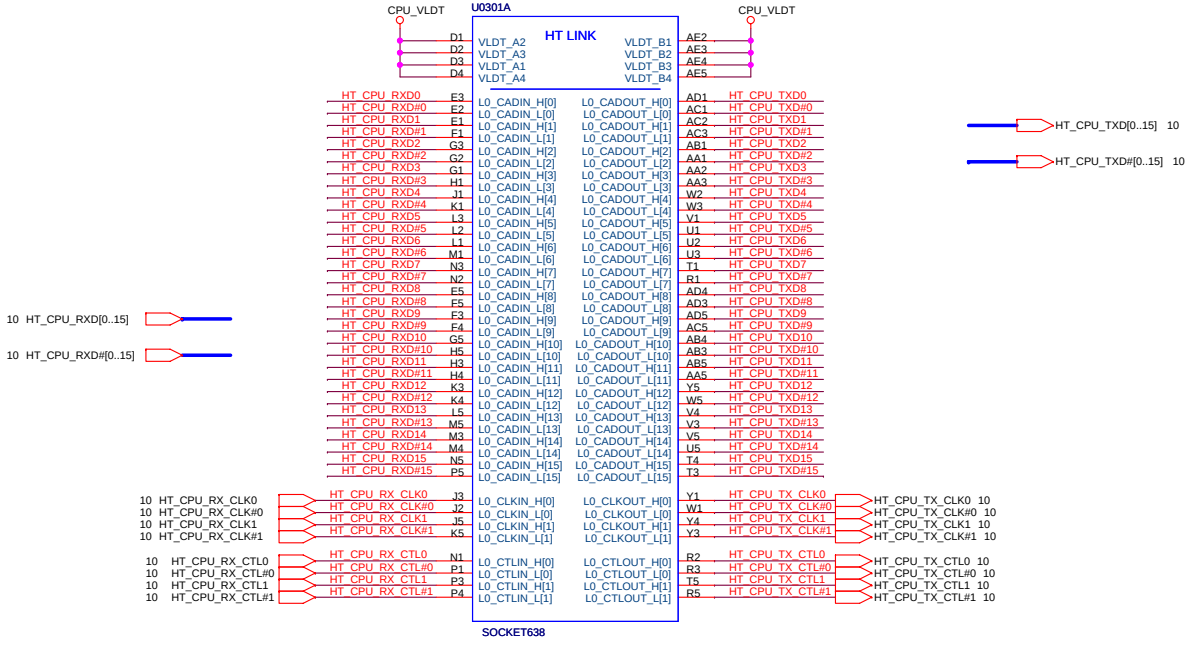
F7Z BLOCK DIAGRAM



<Variant Name>

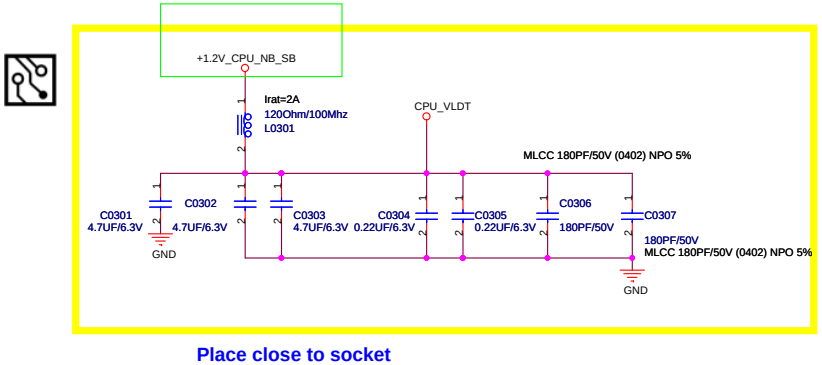
ASUS	Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER INC	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 2.0
Date: Monday, May 19, 2008	Sheet 1 of 94	



12G011306384 071113

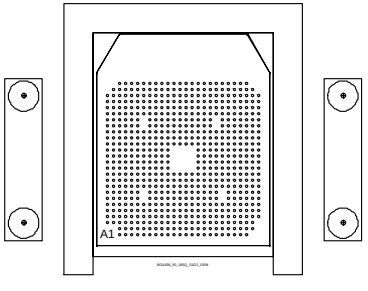
Do not cross plane.

071219 Recover

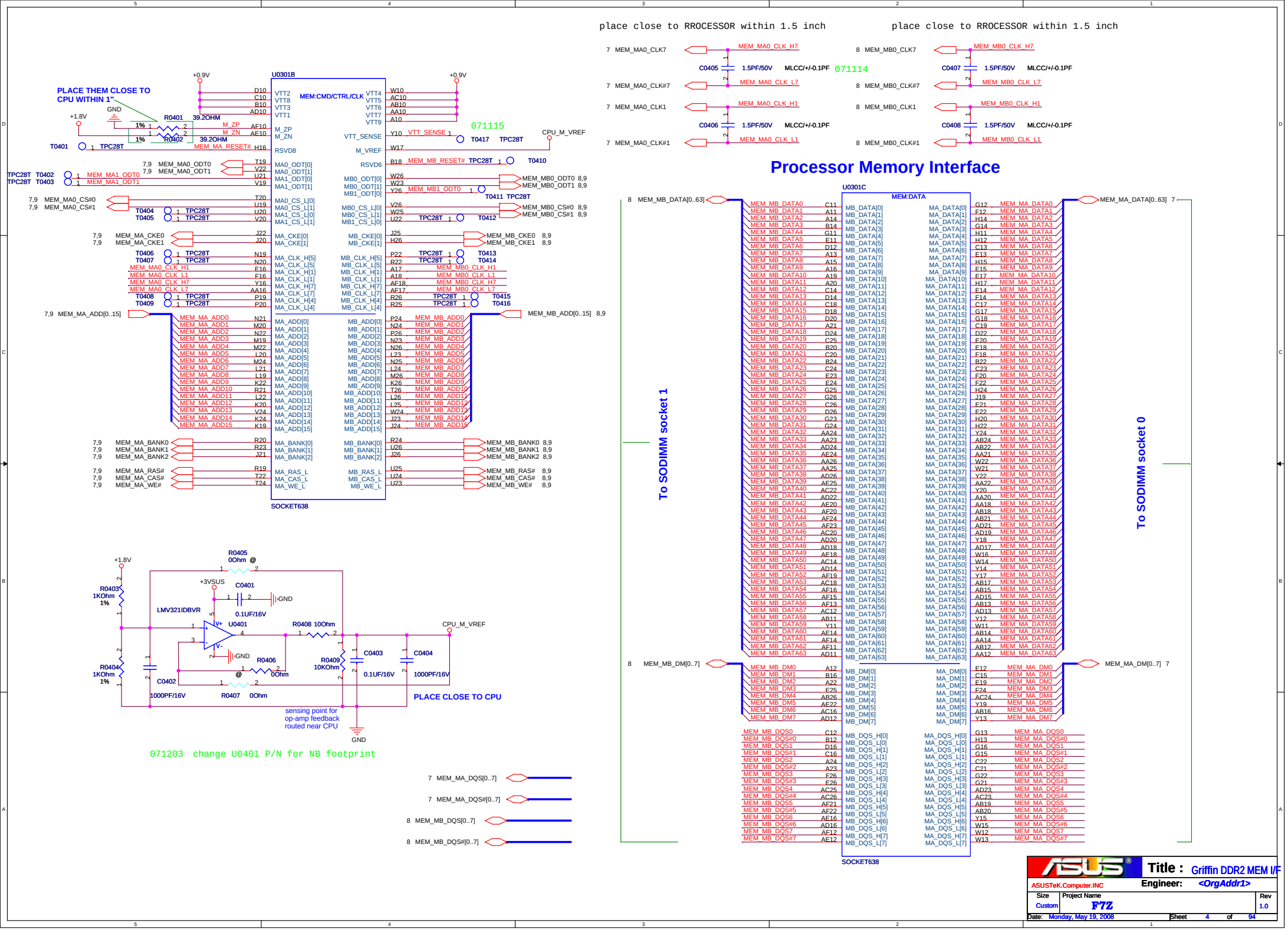


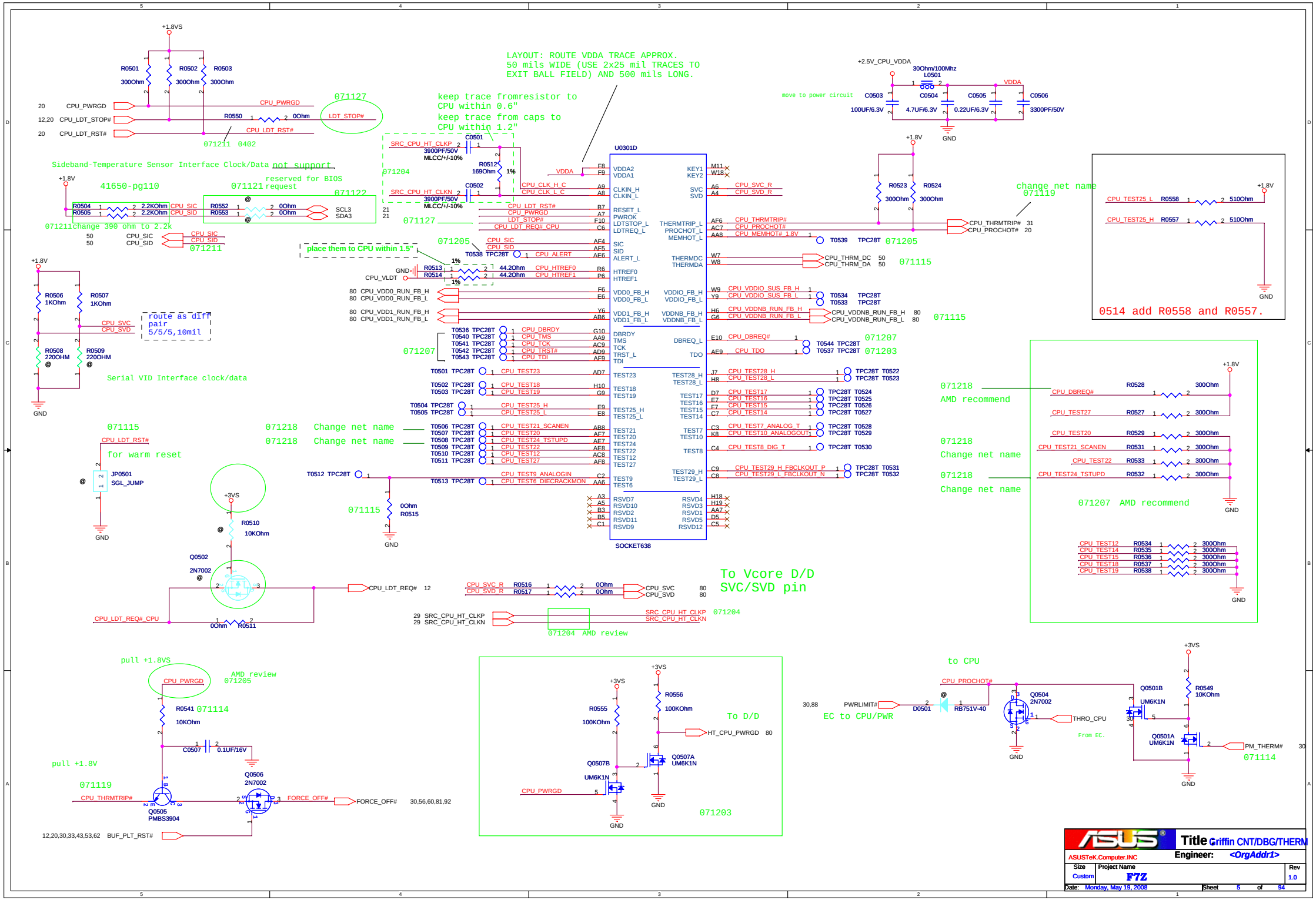
Place close to socket

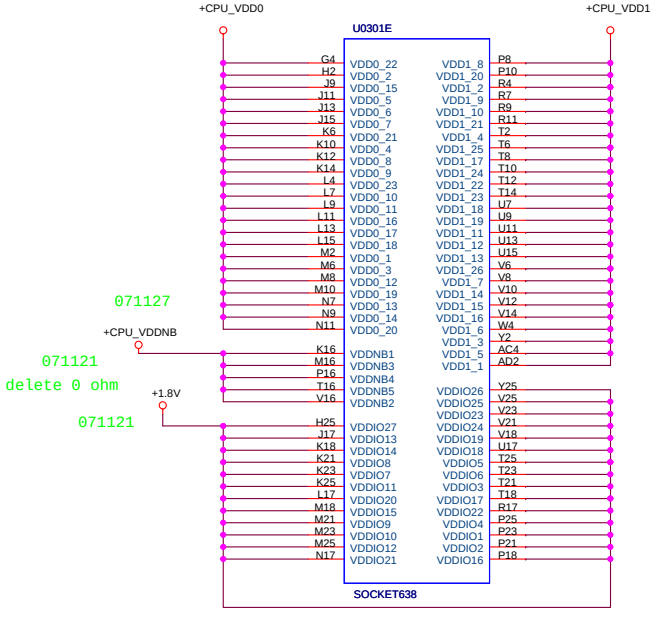
* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side

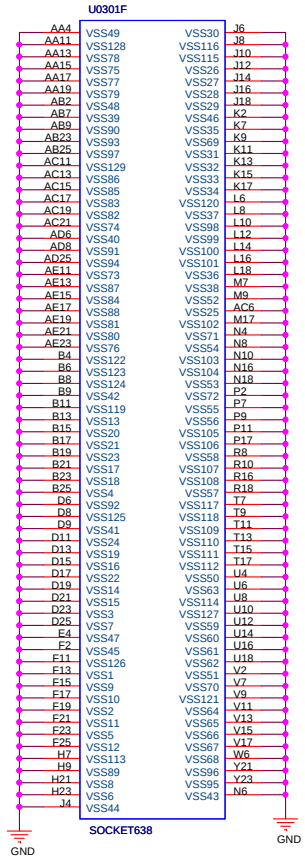


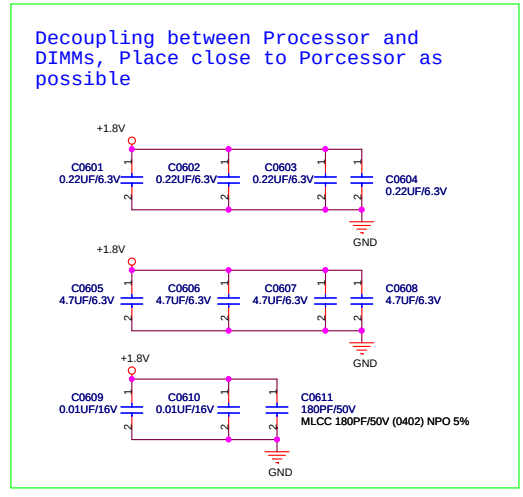
ASUSTeK.Computer.INC	Title : Griffin HT I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 3 of 94		

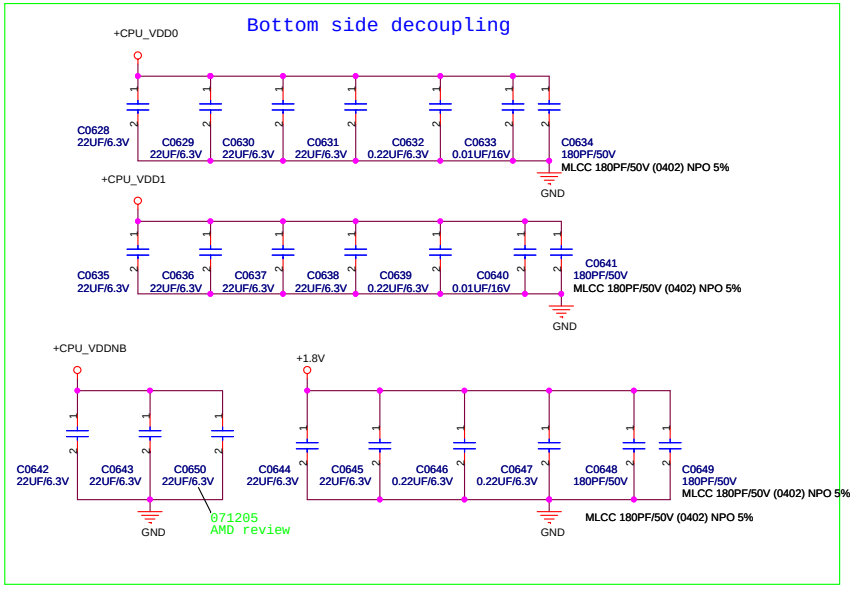

place close to RROCESSOR within 1.5 inch
place close to RROCESSOR within 1.5 inch
7 MEM_MA0_CLK7
MEM_MA0_CLK_H7
C0405 1.5PF/50V MLCC/+/-0.1PF
071114
7 MEM_MA0_CLK#7
MEM_MA0_CLK_L7
7 MEM_MA0_CLK1
MEM_MA0_CLK_H1
C0406 1.5PF/50V MLCC/+/-0.1PF
7 MEM_MA0_CLK#1
MEM_MA0_CLK_L1
8 MEM_MB0_CLK7
MEM_MB0_CLK_H7
C0407 1.5PF/50V MLCC/+/-0.1PF
8 MEM_MB0_CLK#7
MEM_MB0_CLK_L7
8 MEM_MB0_CLK1
MEM_MB0_CLK_H1
C0408 1.5PF/50V MLCC/+/-0.1PF
8 MEM_MB0_CLK#1
MEM_MB0_CLK_L1
Processor Memory Interface
U0301B
MEM:CMD/CTRL/CLK
SOCKET638
PLACE THEM CLOSE TO CPU WITHIN 1"
R0401 39.2OHM
R0402 39.2OHM
T0401 TPC28T
071115
T0417 TPC28T
CPU_M_VREF
T0410
T0411 TPC28T
T0412
T0413
T0414
T0415
T0416
MEM_MB0_ODT0 8,9
MEM_MB0_ODT1 8,9
MEM_MB0_CS#0 8,9
MEM_MB0_CS#1 8,9
MEM_MB_CKE0 8,9
MEM_MB_CKE1 8,9
MEM_MB_ADD[0..15] 8,9
MEM_MB_BANK0 8,9
MEM_MB_BANK1 8,9
MEM_MB_BANK2 8,9
MEM_MB_RAS# 8,9
MEM_MB_CAS# 8,9
MEM_MB_WE# 8,9
U0301C
MEM:DATA
To SODIMM socket 1
To SODIMM socket 0
8 MEM_MB_DATA[0..63]
MEM_MA_DATA[0..63] 7
8 MEM_MB_DM[0..7]
MEM_MA_DM[0..7] 7
SOCKET638
R0405 0Ohm @
+3VSUS
C0401 0.1UF/16V
LMV321IDBVR
U0401
R0403 1KOhm 1%
R0404 1KOhm 1%
R0408 10Ohm
R0406 @ 0Ohm
R0409 10KOhm
C0402 1000PF/16V
R0407 0Ohm
C0403 0.1UF/16V
C0404 1000PF/16V
CPU_M_VREF
PLACE CLOSE TO CPU
sensing point for op-amp feedback routed near CPU
071203 change U0401 P/N for NB footprint
7 MEM_MA_DQS[0..7]
7 MEM_MA_DQS#[0..7]
8 MEM_MB_DQS[0..7]
8 MEM_MB_DQS#[0..7]
Title : Griffin DDR2 MEM I/F
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size Custom
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 4 of 94

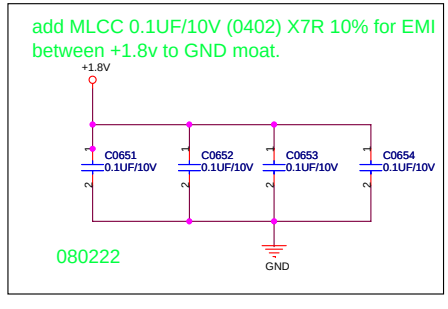

LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"
U0301D
SOCKET638
Sideband-Temperature Sensor Interface Clock/Data not support
41650-pg110
reserved for BIOS request
change net name
071119
0514 add R0558 and R0557.
move to power circuit
Serial VID Interface clock/data
route as diff pair 5/5/5,10mil
place them to CPU within 1.5"
for warm reset
Change net name
AMD recommend
071207 AMD recommend
To Vcore D/D
SVC/SVD pin
071204 AMD review
pull +1.8VS
AMD review
071205
pull +1.8V
EC to CPU/PWR
to CPU
To D/D
ASUSTeK.Computer.INC
Title Griffin CNT/DBG/THERM
Engineer: <OrgAddr1>
Size Custom
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 5 of 94

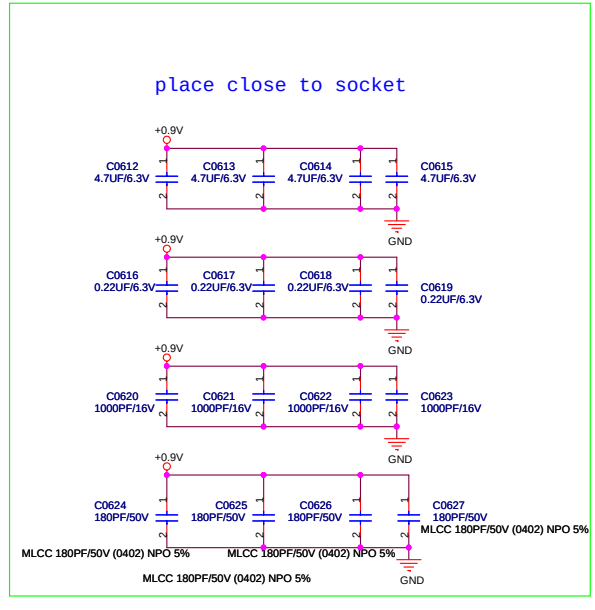






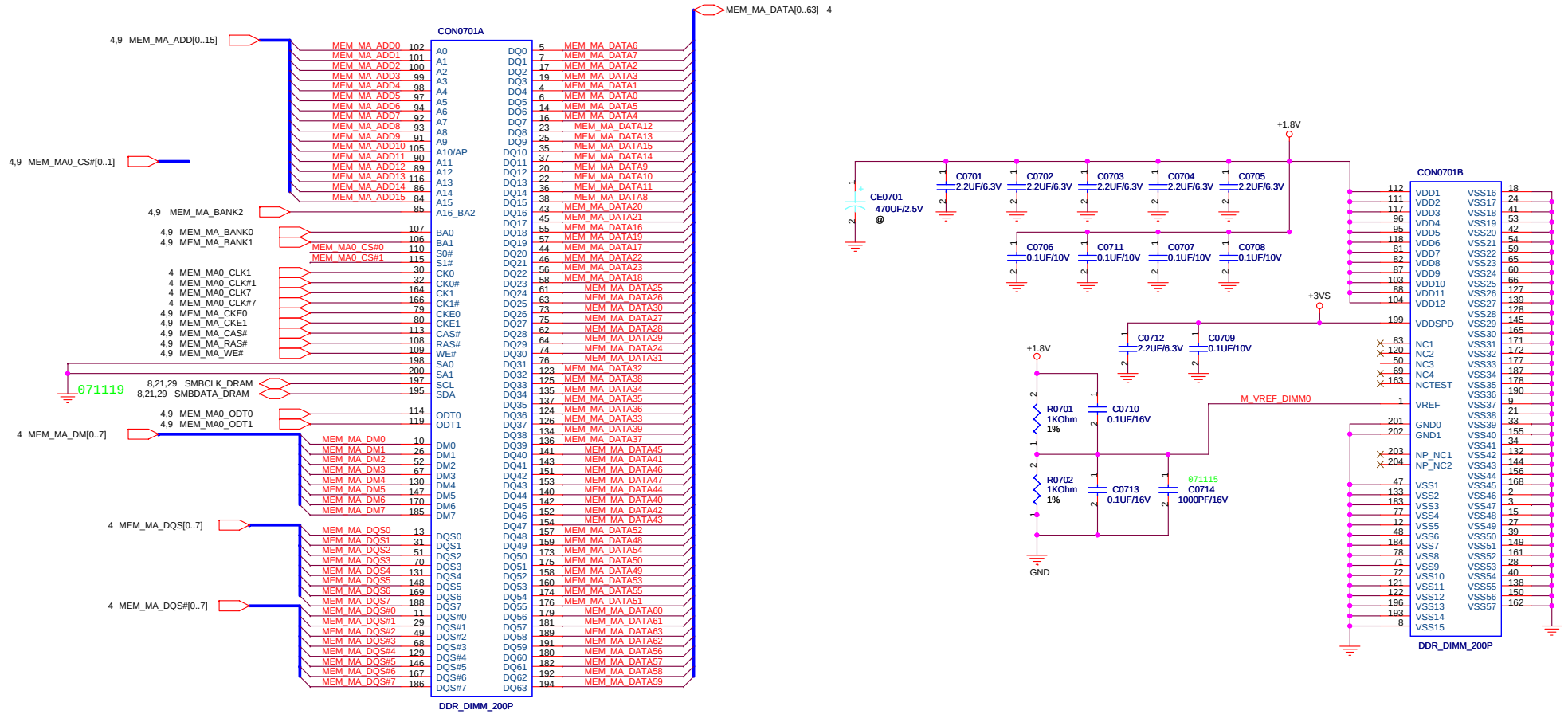






ASUSTeK.Computer.INC	Title : Griffin Power	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 6 of 94	

080220
SWAP



PN:12G025122006

modify 05/24

<Variant Name>

ASUSTeK COMPUTER INC

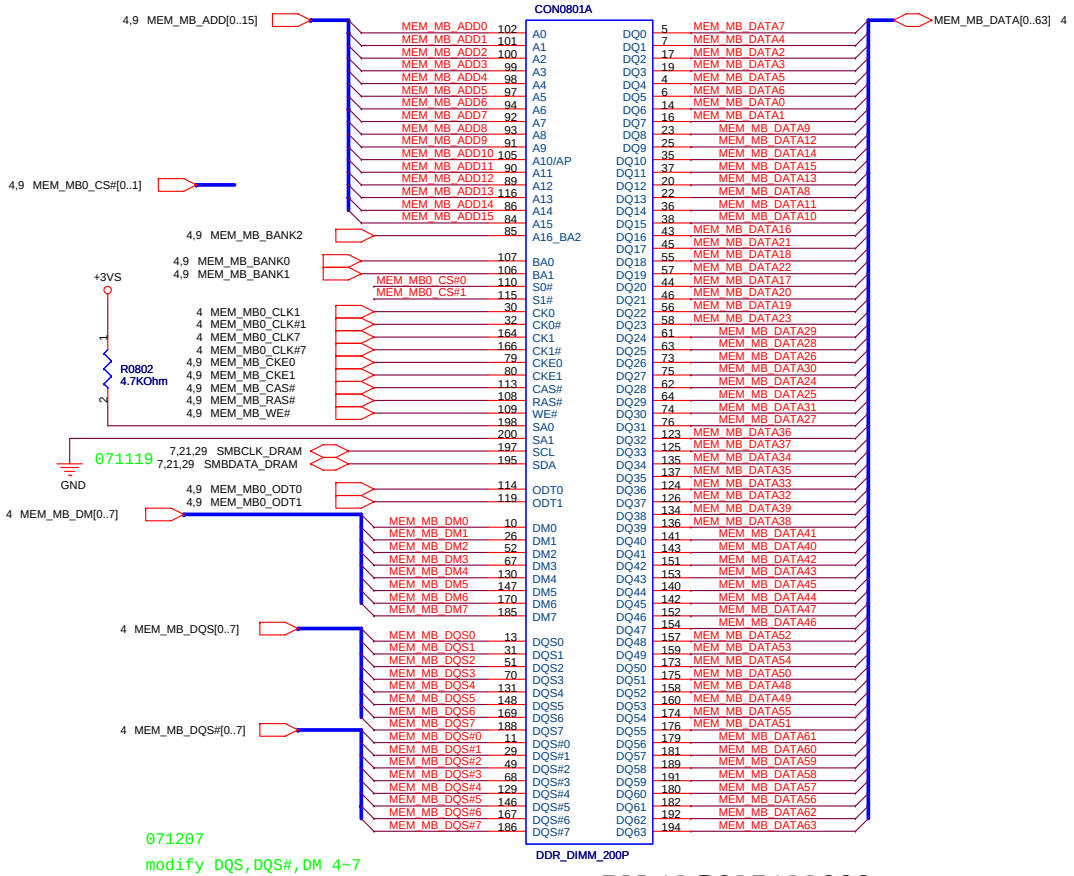
Title : DDR2 SO-DIMM0

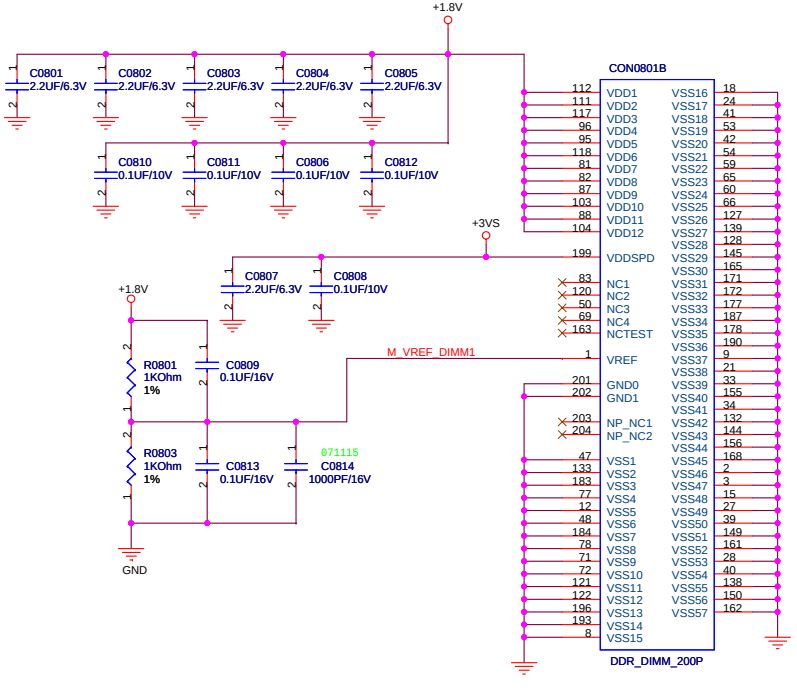
Engineer:

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 7 of 94

080221
SWAP

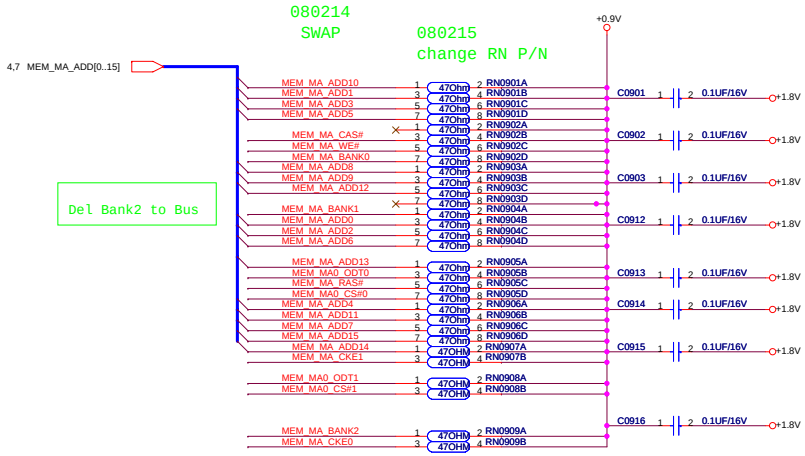


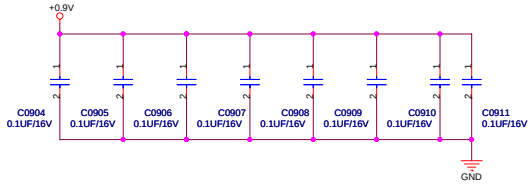


071207
modify DQS,DQS#,DM 4~7

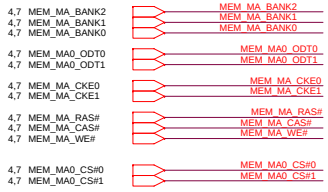
PN:12G025122000

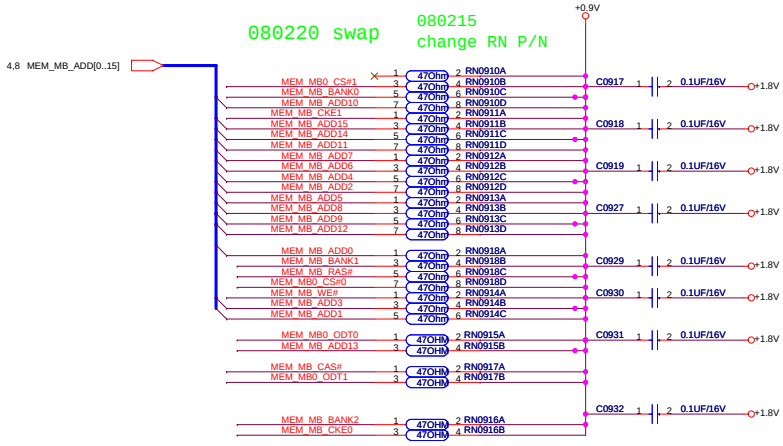
ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM1	
	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 8 of 94	

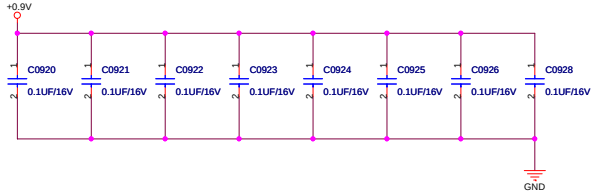




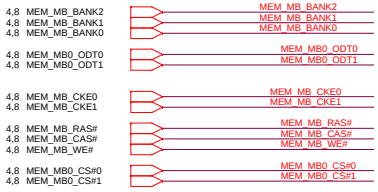
071207

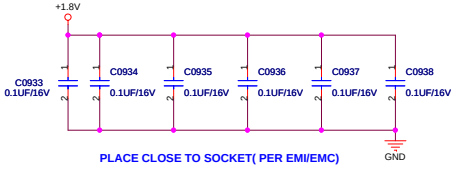






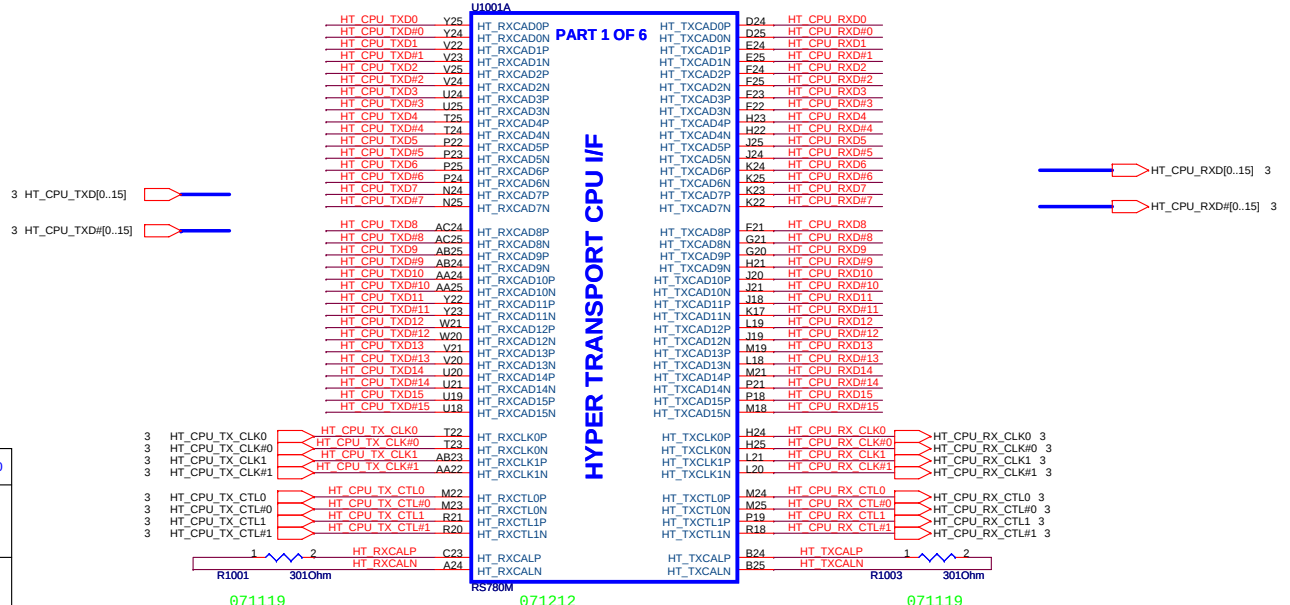
071211





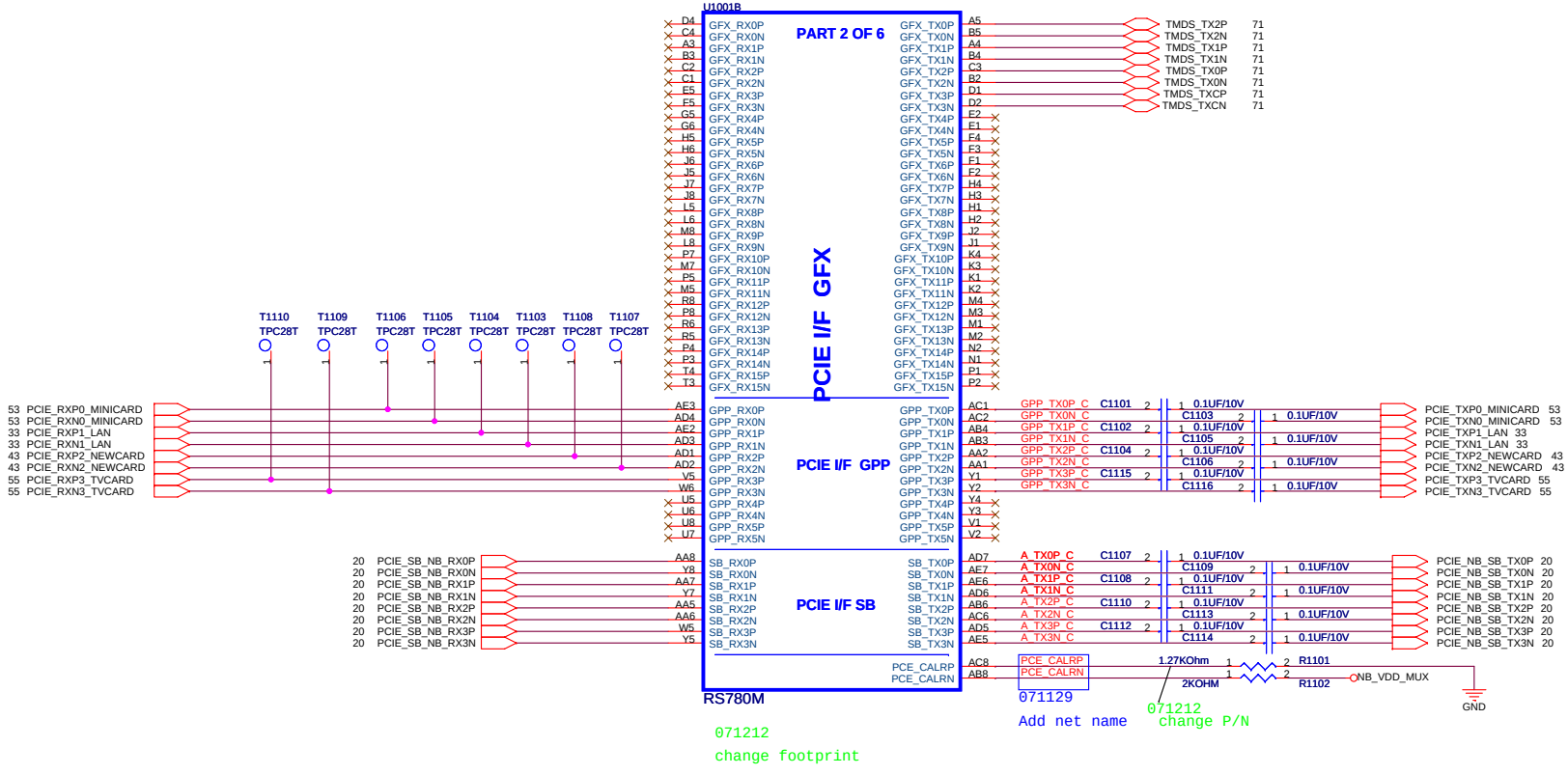
PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC	Title : DDR2_TERMINATIONS		
	Engineer:		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 9 of 94		



Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

ASUS	Title : RS780M-HT LINK I/F		
ASUSTeK.Computer.INC	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 10 of 94		



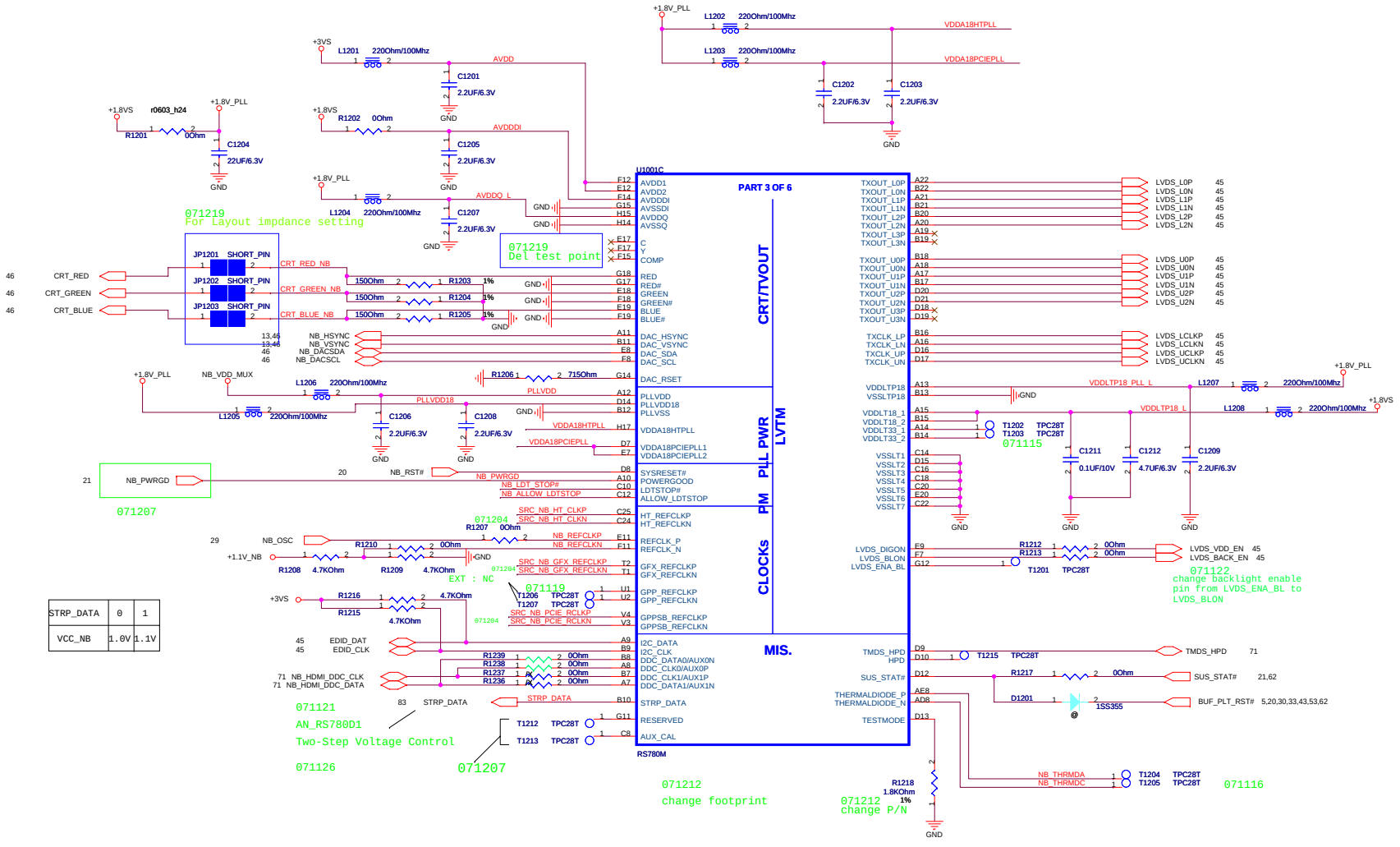
ASUSTeK.Computer.INC

Title : RS780M-PCIE LINK I/F

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F7Z	1.0

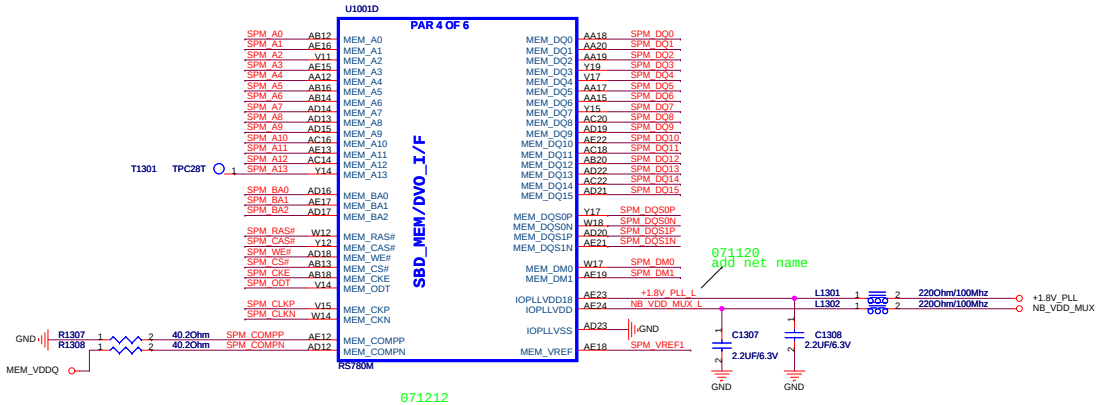
Date: Monday, May 19, 2008 Sheet 11 of 94



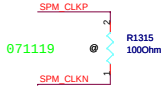
STRP_DATA	0	1
VCC_NB	1.0V	1.1V

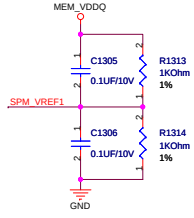
ASUSTeK.Computer.INC	Title : RS780M-SYS I/F		
	Engineer: <OrgAddr1>		
Size C	Project Name F7Z		Rev 1.0
Date: Monday, May 19, 2008	Sheet 12 of 94		

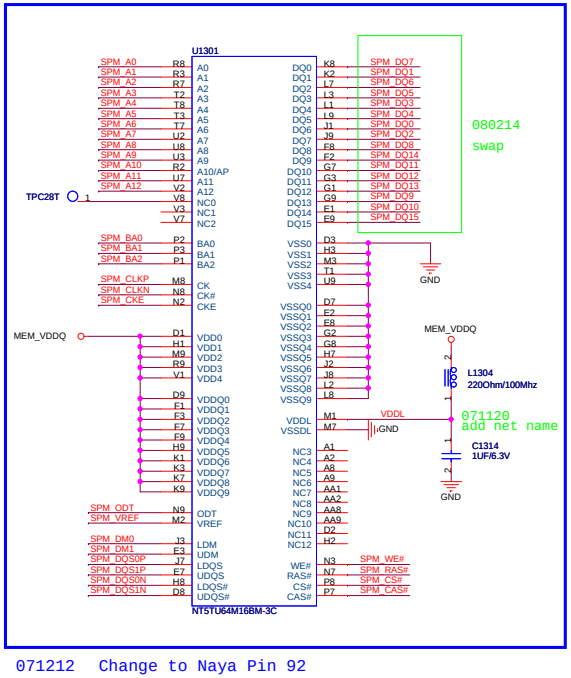
071113

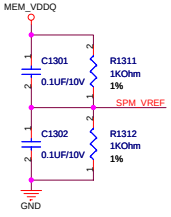


071212
change footprint









071212 Change to Naya Pin 92

071218

AMD Qualified

16Mx16 Hynix HY5PS561621AFP-25 asus P/N: 03G151236214

32Mx16 Qimonda HYB18T512161B2F-25 asus P/N :03G15133F211

64Mx16 Samsung K4N16164QQ-HC25 asus P/N -

F5Z Use

DFT_GPIO1: LOAD_EEPROM_STRAPS

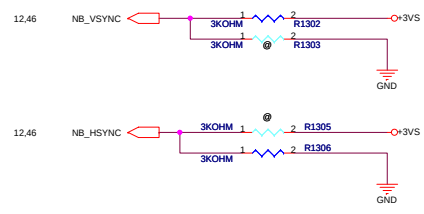
```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

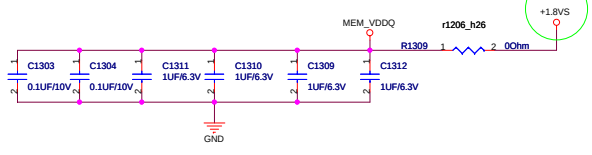
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

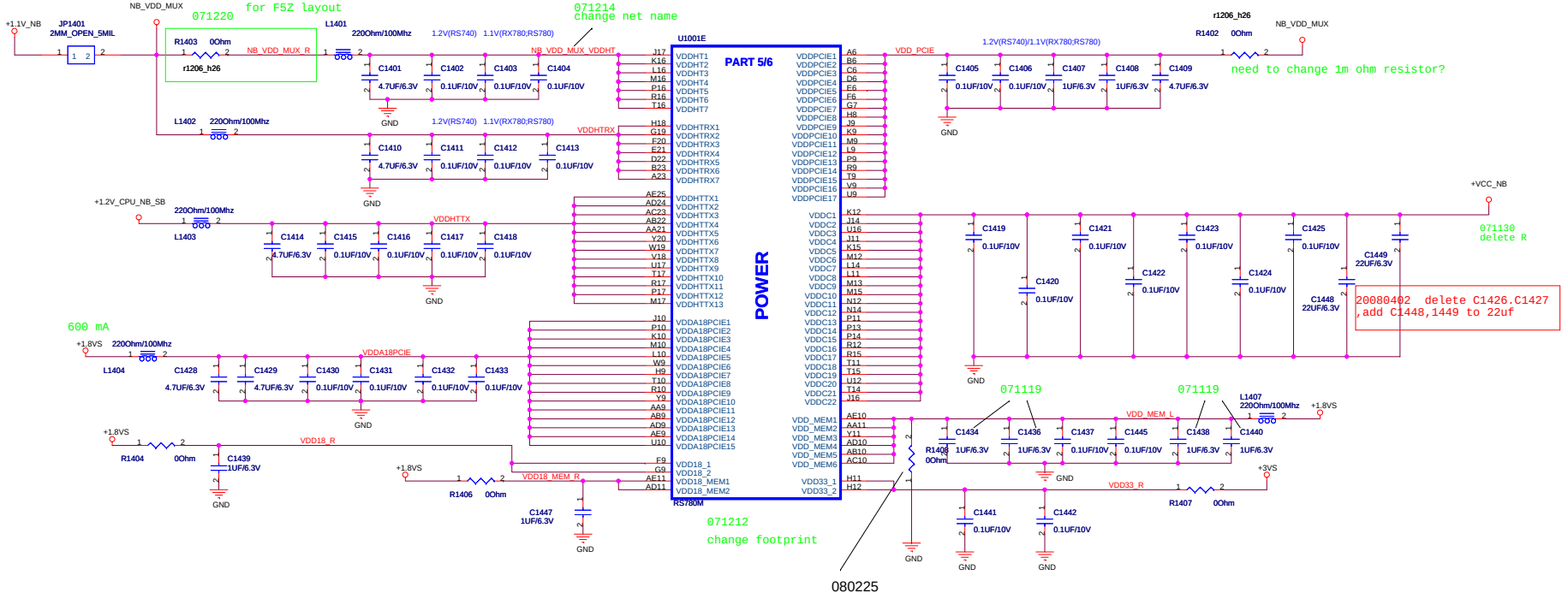
```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

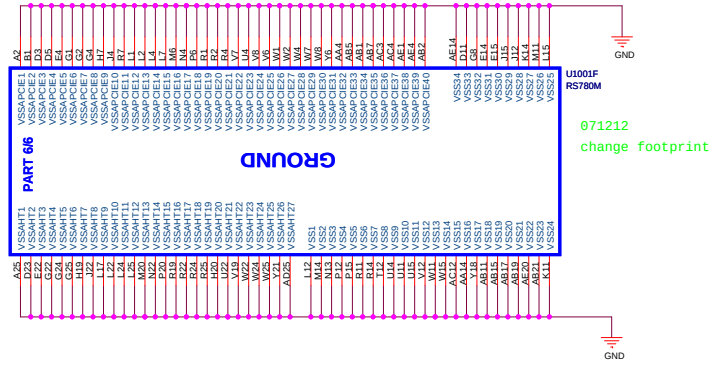


071119

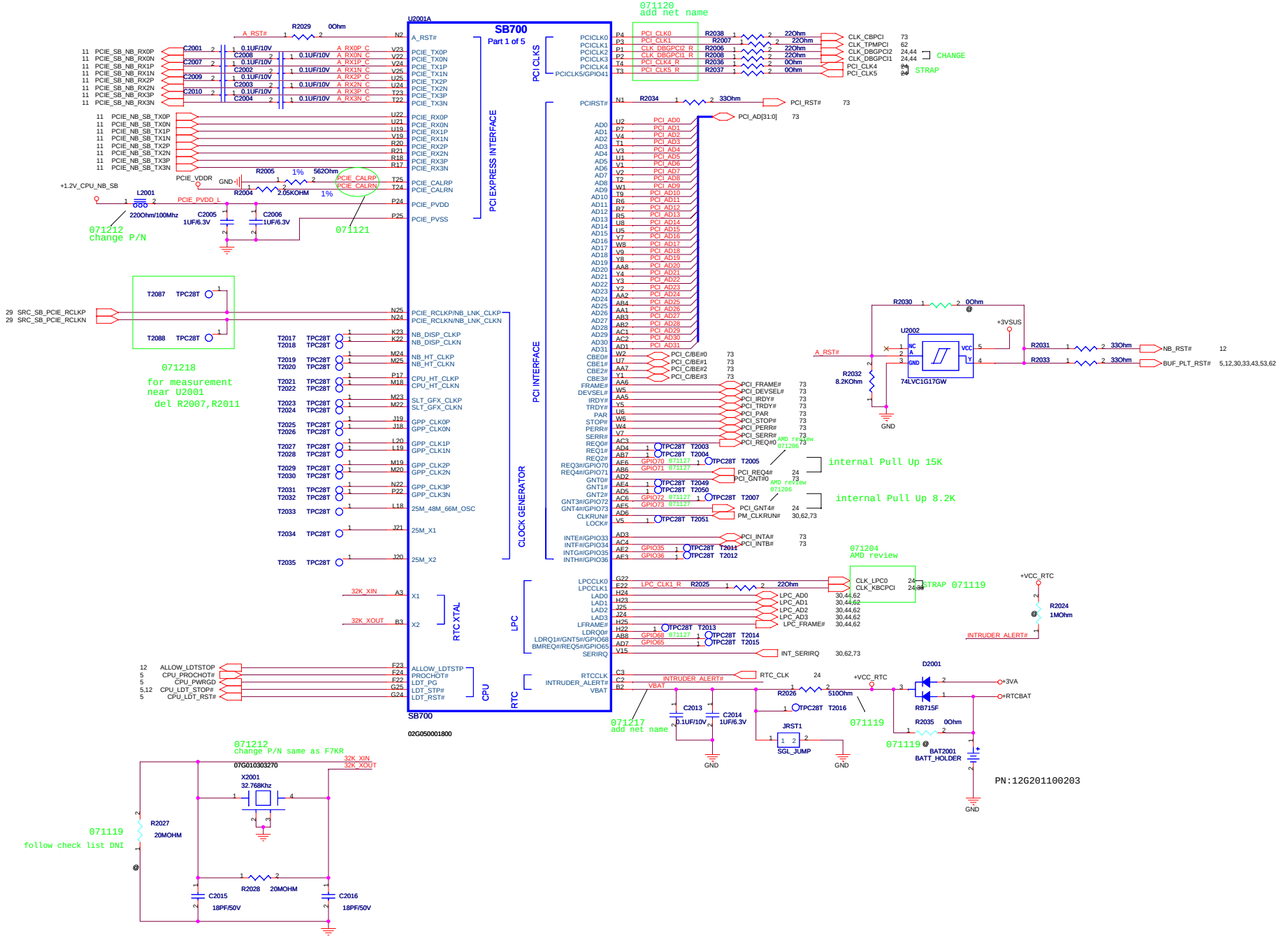


ASUS ASUSTeK.Computer.INC	Title : RS780M-SPMEM/STRAP	
	Engineer: <OrgAddr1>	
Size C	Project Name F7Z	Rev 1.0
Date: Monday, May 19, 2008	Sheet 13 of 94	

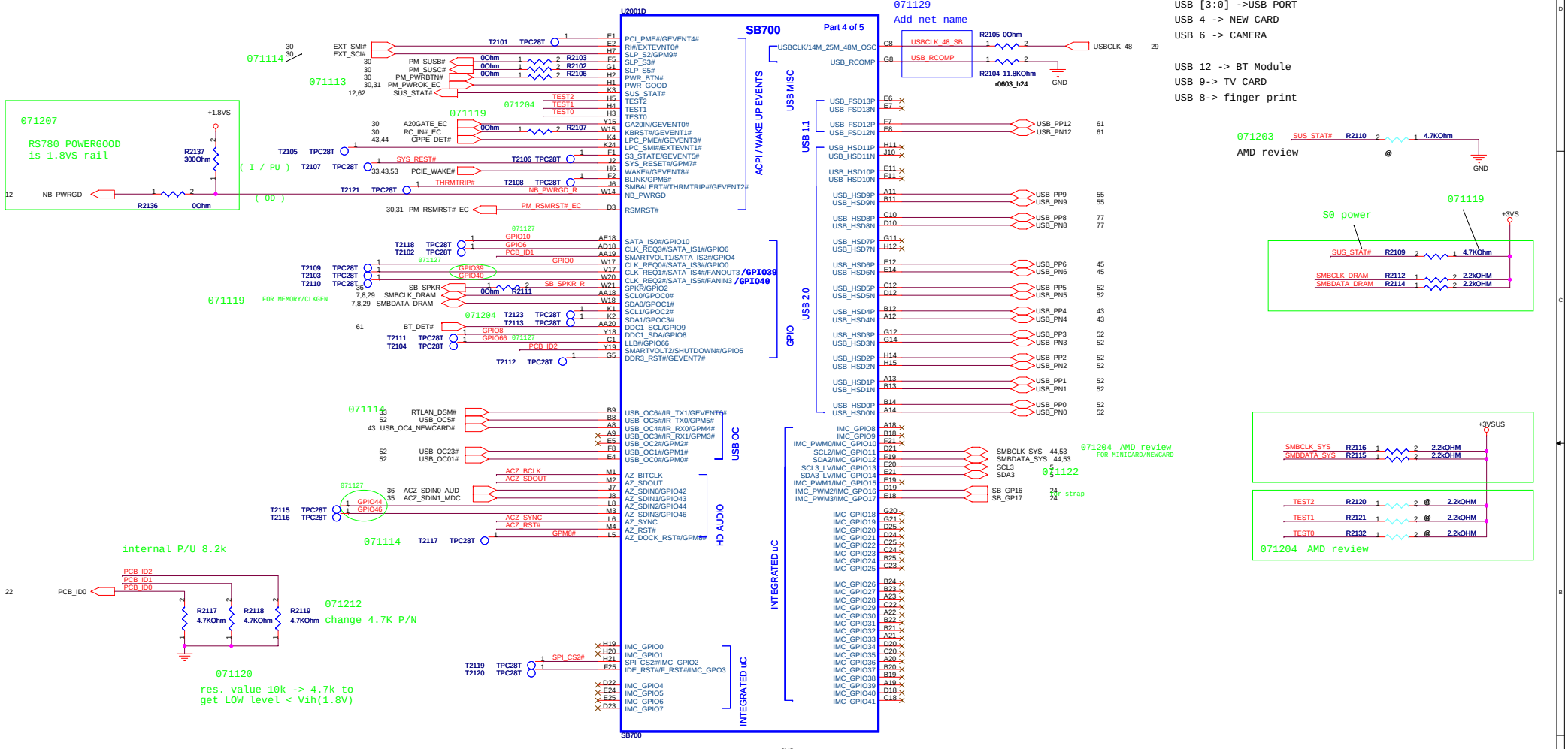


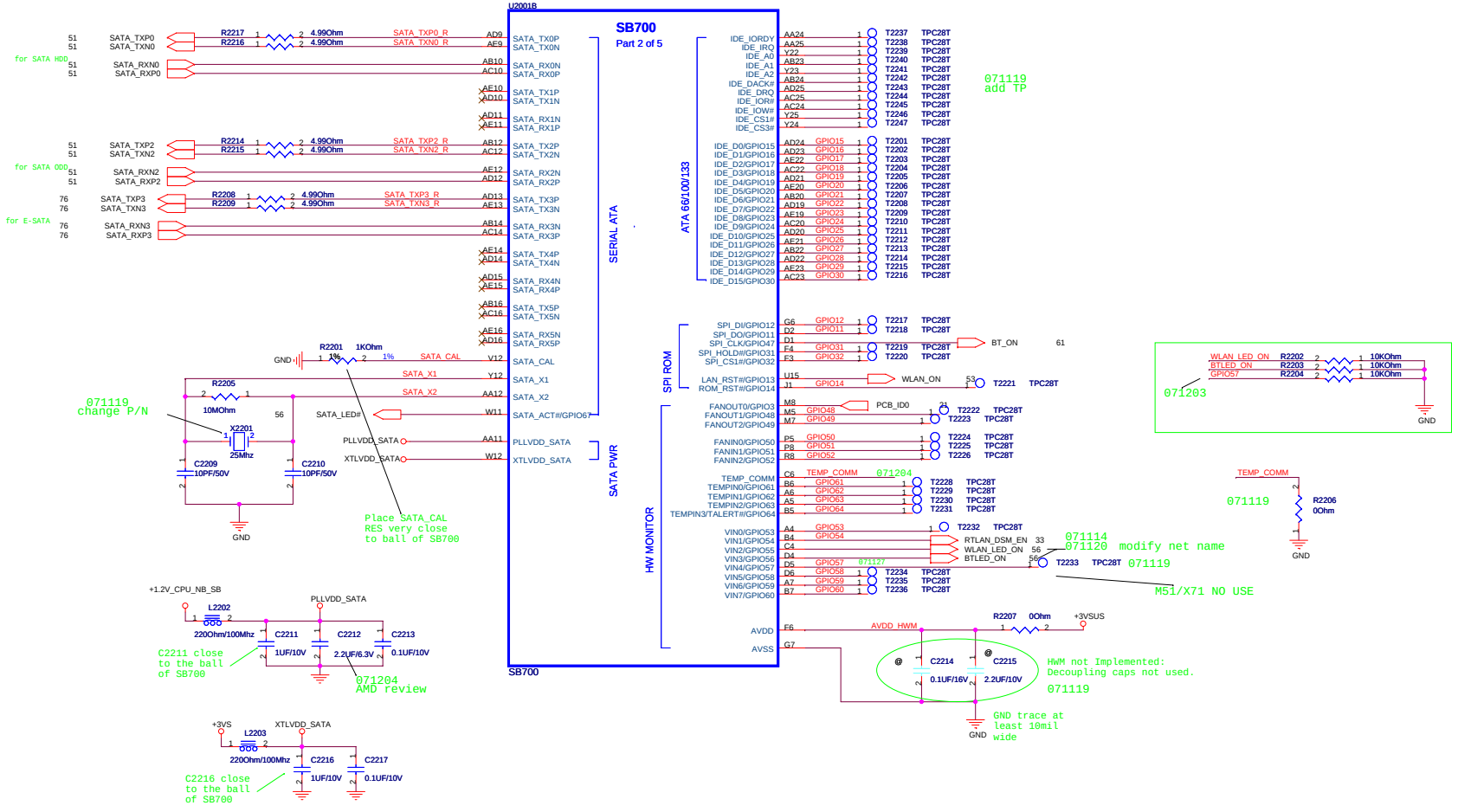


ASUSTeK.Computer.INC	Title : RS780M-POWER	
	Engineer: <OrgAddr1>	
Size C	Project Name F7Z	Rev 1.0
Date: Monday, May 19, 2008	Sheet 14 of 94	

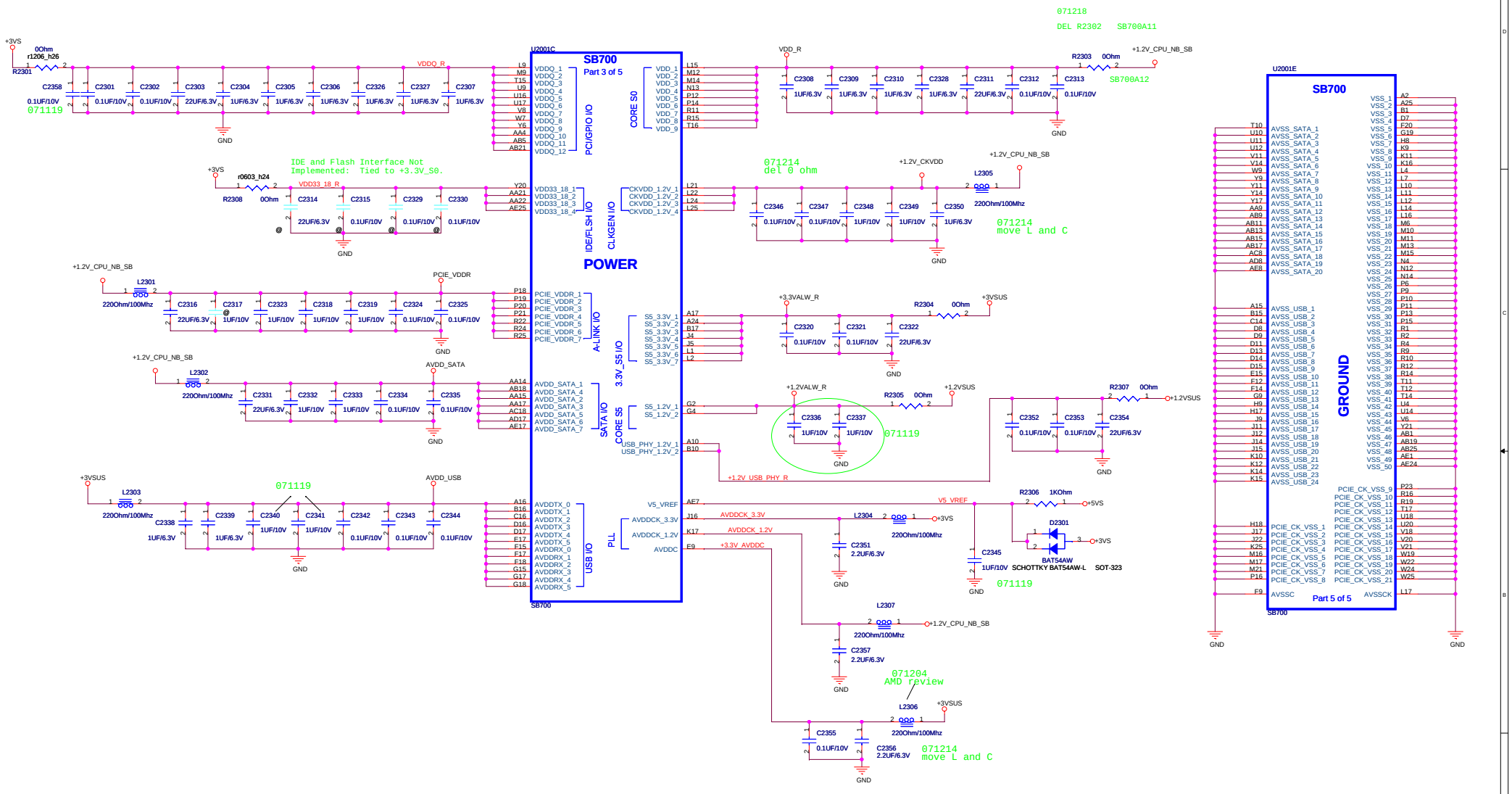


ASUSTeK.Computer.INC	Title : SB700_CPU/PCIE/LPC/CLK
	Engineer: <OrgAddr1>
Size: C	Project Name: F7Z
Rev: 1.0	
Date: Monday, May 19, 2008	Sheet 20 of 94

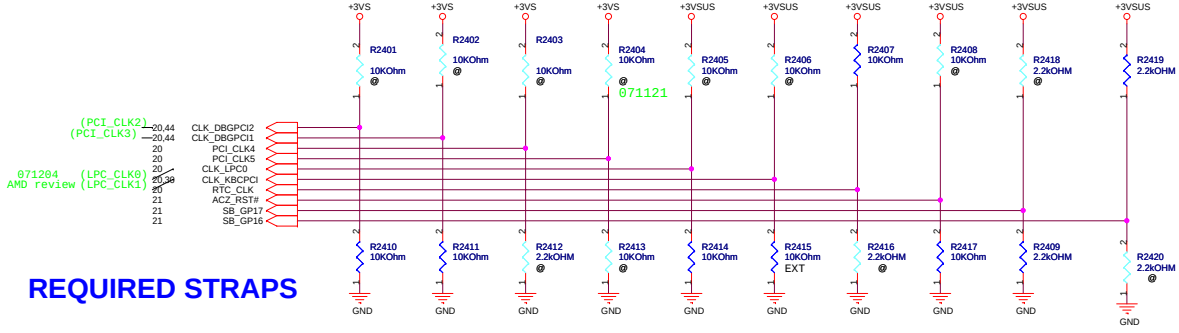

SB700
Part 4 of 5
U2001D
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
071129
Add net name
USB5->USB PORT
USB [3:0] ->USB PORT
USB 4 -> NEW CARD
USB 6 -> CAMERA
USB 12 -> BT Module
USB 9-> TV CARD
USB 8-> finger print
071207
RS780 POWERGOOD
is 1.8VS rail
071203
AMD review
S0 power
071119
071114
071113
071204
071122
071212
change 4.7K P/N
internal P/U 8.2k
071120
res. value 10k -> 4.7k to
get LOW level < Vih(1.8V)
071204 AMD review
for strap
SB700A11
SB700A13
PUT AT SB700 SIDE
080402
AMD review
need to modify topology??
Title : SB700_GPIO/USB/HD/ACPI
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 21 of 94



ASUSTeK.Computer.INC	Title : SB700_PATA/SATA		
	Engineer: <OrgAddr1>		
Size C	Project Name F7Z		Rev 1.0
Date: Monday, May 19, 2008	Sheet 22 of 94		


SB700
Part 3 of 5
POWER
U2001C
071218
DEL R2302 SB700A11
SB700A12
071119
IDE and Flash Interface Not
Implemented: Tied to +3.3V_S0.
071214
del 0 ohm
071214
move L and C
071204
AMD review
U2001E
SB700
GROUND
Part 5 of 5
Title : SB700_POWER
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 23 of 94

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

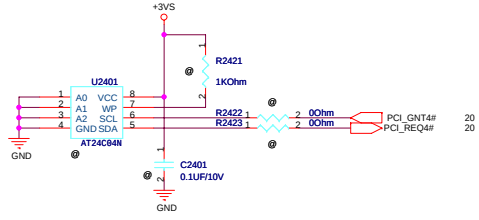


REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

071206
AMD review



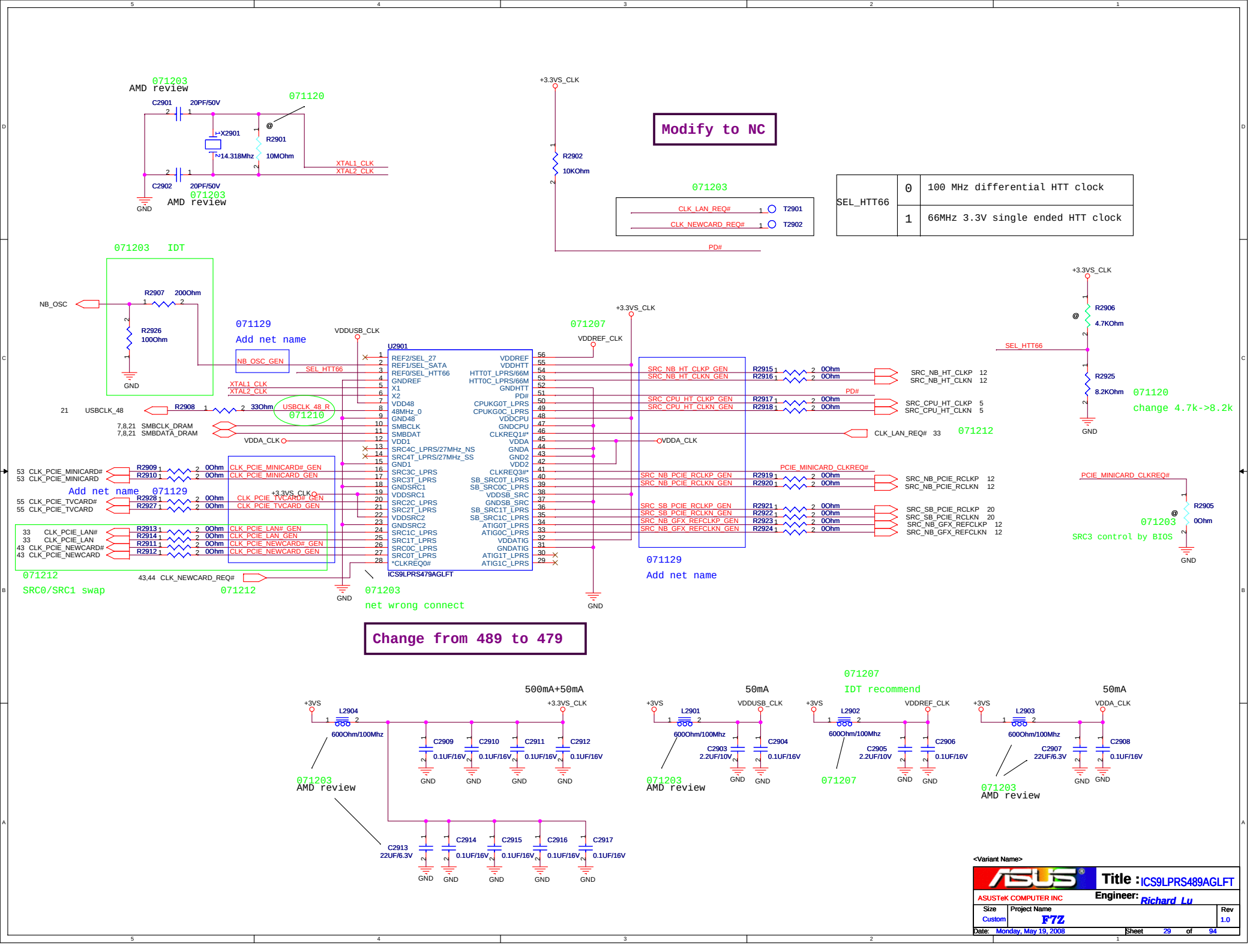
ASUSTeK.Computer.INC

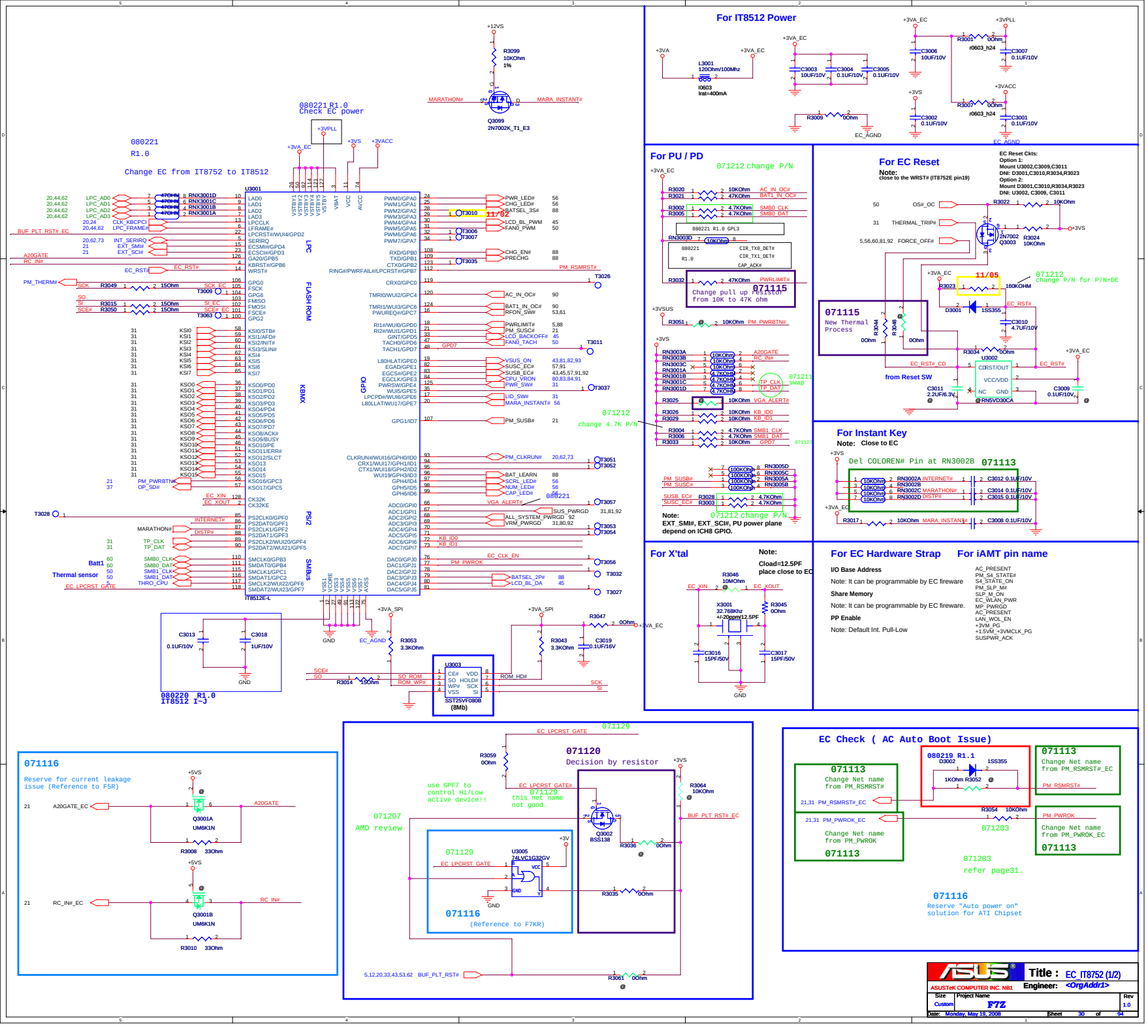
Title : SB700_STRAP

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 24 of 94

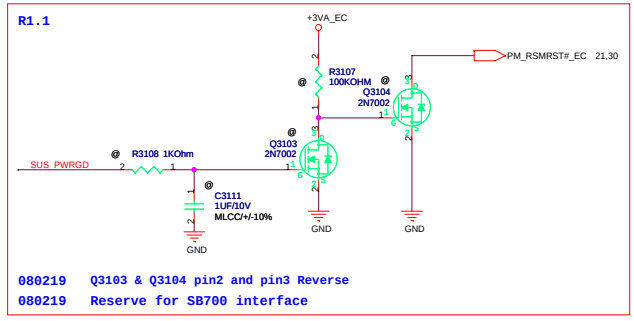

071203
AMD review
C2901
20PF/50V
071120
X2901
14.318Mhz
R2901
10MOhm
XTAL1_CLK
XTAL2_CLK
C2902
20PF/50V
071203
AMD review
GND
+3.3VS_CLK
R2902
10KOhm
Modify to NC
071203
CLK_LAN_REQ#
CLK_NEWCARD_REQ#
T2901
T2902
PD#
SEL_HTT66
0 100 MHz differential HTT clock
1 66MHz 3.3V single ended HTT clock
071203 IDT
NB_OSC
R2907 200Ohm
R2926 100Ohm
071129
Add net name
NB_OSC_GEN
VDDUSB_CLK
U2901
071207
VDDREF_CLK
+3.3VS_CLK
XTAL1_CLK
XTAL2_CLK
21 USBCLK_48
R2908 33Ohm
USBCLK_48_R
071210
7,8,21 SMBCLK_DRAM
7,8,21 SMBDATA_DRAM
VDDA_CLK
53 CLK_PCIE_MINICARD#
53 CLK_PCIE_MINICARD
R2909 0Ohm CLK_PCIE_MINICARD# GEN
R2910 0Ohm CLK_PCIE_MINICARD GEN
Add net name 071129
55 CLK_PCIE_TVCARD#
55 CLK_PCIE_TVCARD
R2928 0Ohm CLK_PCIE_TVCARD# GEN
R2927 0Ohm CLK_PCIE_TVCARD GEN
+3.3VS_CLK
33 CLK_PCIE_LAN#
33 CLK_PCIE_LAN
43 CLK_PCIE_NEWCARD#
43 CLK_PCIE_NEWCARD
R2913 0Ohm CLK_PCIE_LAN# GEN
R2914 0Ohm CLK_PCIE_LAN GEN
R2911 0Ohm CLK_PCIE_NEWCARD# GEN
R2912 0Ohm CLK_PCIE_NEWCARD GEN
071212
SRC0/SRC1 swap
43,44 CLK_NEWCARD_REQ#
071212
GND
071203
net wrong connect
REF2/SEL_27
REF1/SEL_SATA
REF0/SEL_HTT66
GNDREF
X1
X2
VDD48
48MHz_0
GND48
SMBCLK
SMBDAT
VDD1
SRC4C_LPRS/27MHz_NS
SRC4T_LPRS/27MHz_SS
GND1
SRC3C_LPRS
SRC3T_LPRS
GNDSRC1
VDDSRC1
SRC2C_LPRS
SRC2T_LPRS
VDDSRC2
GNDSRC2
SRC1C_LPRS
SRC1T_LPRS
SRC0C_LPRS
SRC0T_LPRS
*CLKREQ0#
VDDREF
VDDHTT
HTT0T_LPRS/66M
HTT0C_LPRS/66M
GNDHTT
PD#
CPUKG0T_LPRS
CPUKG0C_LPRS
VDDCPU
GNDCPU
CLKREQ1#*
VDDA
GNDA
GND2
VDD2
CLKREQ3#*
SB_SRC0T_LPRS
SB_SRC0C_LPRS
VDDSB_SRC
GNDSB_SRC
SB_SRC1T_LPRS
SB_SRC1C_LPRS
ATIG0T_LPRS
ATIG0C_LPRS
VDDATIG
GNDATIG
ATIG1T_LPRS
ATIG1C_LPRS
ICS9LPRS479AGLFT
SRC_NB_HT_CLKP_GEN
SRC_NB_HT_CLKN_GEN
R2915 0Ohm
R2916 0Ohm
SRC_NB_HT_CLKP 12
SRC_NB_HT_CLKN 12
SRC_CPU_HT_CLKP_GEN
SRC_CPU_HT_CLKN_GEN
R2917 0Ohm
R2918 0Ohm
SRC_CPU_HT_CLKP 5
SRC_CPU_HT_CLKN 5
CLK_LAN_REQ# 33
071212
PCIE_MINICARD_CLKREQ#
SRC_NB_PCIE_RCLKP_GEN
SRC_NB_PCIE_RCLKN_GEN
R2919 0Ohm
R2920 0Ohm
SRC_NB_PCIE_RCLKP 12
SRC_NB_PCIE_RCLKN 12
SRC_SB_PCIE_RCLKP_GEN
SRC_SB_PCIE_RCLKN_GEN
SRC_NB_GFX_REFCLKP_GEN
SRC_NB_GFX_REFCLKN_GEN
R2921 0Ohm
R2922 0Ohm
R2923 0Ohm
R2924 0Ohm
SRC_SB_PCIE_RCLKP 20
SRC_SB_PCIE_RCLKN 20
SRC_NB_GFX_REFCLKP 12
SRC_NB_GFX_REFCLKN 12
071129
Add net name
+3.3VS_CLK
R2906 4.7KOhm
SEL_HTT66
R2925 8.2KOhm
071120
change 4.7k->8.2k
PCIE_MINICARD_CLKREQ#
R2905 0Ohm
071203
SRC3 control by BIOS
Change from 489 to 479
500mA+50mA
+3.3VS_CLK
+3VS
L2904
600Ohm/100Mhz
C2909 0.1UF/16V
C2910 0.1UF/16V
C2911 0.1UF/16V
C2912 0.1UF/16V
071203
AMD review
C2913 22UF/6.3V
C2914 0.1UF/16V
C2915 0.1UF/16V
C2916 0.1UF/16V
C2917 0.1UF/16V
50mA
VDDUSB_CLK
L2901
600Ohm/100Mhz
C2903 2.2UF/10V
C2904 0.1UF/16V
071203
AMD review
071207
IDT recommend
VDDREF_CLK
L2902
600Ohm/100Mhz
C2905 2.2UF/10V
C2906 0.1UF/16V
071207
50mA
VDDA_CLK
L2903
600Ohm/100Mhz
C2907 22UF/6.3V
C2908 0.1UF/16V
071203
AMD review
GND
<Variant Name>
ASUSTeK COMPUTER INC
Title : ICS9LPRS489AGLFT
Engineer: Richard_Lu
Size Custom
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 29 of 94


For IT8512 Power
For PU / PD
For EC Reset
For Instant Key
For X'tal
For EC Hardware Strap
For iAMT pin name
EC Check (AC Auto Boot Issue)
080221 R1.0
Check EC power
080221
R1.0
Change EC from IT8752 to IT8512
080220 R1.0
IT8512 I~J
071212 change P/N
071212 change P/N for P/N+DE
071212 change 4.7K P/N
071212 change P/N
071115
Change pull up resistor from 10K to 47K ohm
071115
New Thermal Process
071113
Del COLOREN# Pin at RN3002B
071116
Reserve for current leakage issue (Reference to FSR)
071120
Decision by resistor
071129
071207
AMD review
071203
refer page31.
071116
Reserve "Auto power on" solution for ATI Chipset
Title : EC_IT8752 (1/2)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size: Custom
Project Name: F7Z
Rev: 1.0
Date: Monday, May 19, 2008
Sheet 30 of 94

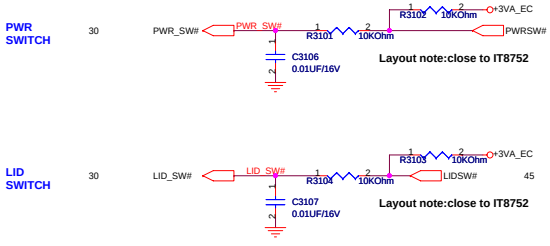
For Battery

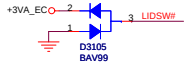
Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

In Page 60



For Switch

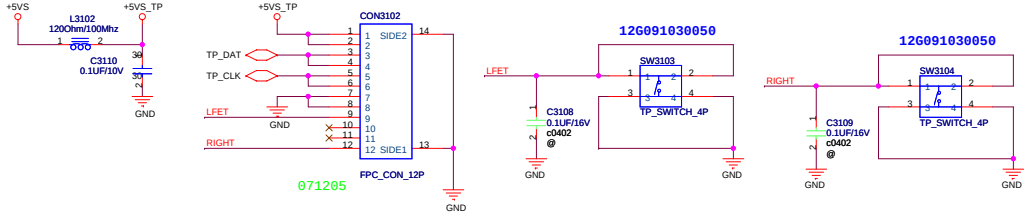




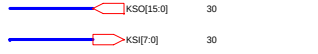
close to connector

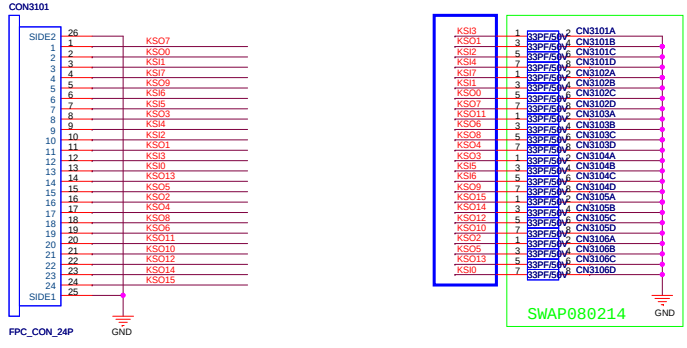
Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

Touch-Pad (F7se)

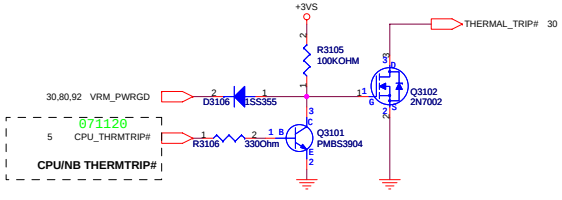


Keyboard Connector (F7se)





For Thermal Control Method



ASUSTeK COMPUTER INC. NB1

Title : EC_IT8511 (2/2)

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 31 of 94

ALL Follow Design IP

071119 Add net name

+VDD33 R3302 0Ohm r0805_h24 VDDSR C3306 22UF/6.3V C3305 0.1UF/10V 40 mil GND

071212 change P/N

CONNECT TO 3.3V ENABLE ;0V TO DISABLE SWIRTCHING REGULATOR

close to pin63 within 200 mil

close to pin64

R3305 2.49KOhm GND

XIN_LAN XOUT_LAN +AVDD33 +AVDD12

Add net name

VCTRL12 071113 L3301 4.7UH 60 mil

close to pin1 with in 200 mil please change:09G02X473522 4.7uH/20% close to L3301 with in 200 mil

C3307 22UF/6.3V C3309 0.1UF/10V GND

071212 change P/N

close to IC 200 mil

0Ohm R3301 FB12 +V1.2

L3304 80Ohm/100Mhz L3303 80Ohm/100Mhz

071130 Add L3304

C3301 C3302 C3303 C3304 0.1UF/10V GND +AVDD12 +EVDD12

C3308 C3311 0.1UF/10V GND_AGND_A

071130 Add R3318

R3318 0Ohm 40mil +VDD12

C3310 C3313 C3314 C3315 C3316 C3317 0.1UF/10V GND

Add DSM function

Reserved DSM Function

R3319 0Ohm RTLAN_DSM# 21 RTLAN_DSM_EN 22

Change to 2N7002

+3VS R3307 1KOhm Q3301 2N7002 GND

@ R3317 1% 100Ohm

R3309 15KOhm GND

+VDD12 +VDD33 T3301

+AVDD12 +AVDD33

U3301 RTL8111C_VB_GR

GND RSET VDDSR ENSR CKTAL2 CKTAL1 AVDD33_2 AVDD12_4 LED0 LED1 LED2 LED3 VDD33_4 DVDD12_6 OGPIO IGPIO DVDD12_5

SROUT12 AVDD33_1 MDIP0 MDIN0 FB12 MDIP1 MDIN1 AVDD12_1 MDIP2 MDIN2 AVDD12_2 MDIP3 MDIN3 AVDD12_3 NC1 VDD33_1

EESK EEDI/AUX VDD33_3 EEDO EECS DVDD12_4 NC9 NC8 NC7 NC6 DVDD12_3 VDD33_2 ISOLATEB NC5 NC4 CLKREQB

NC2 NC3 LANWAKEB PERSTB DVDD12_1 EVDD12_1 HSIP HSIN EGND1 REFCLK_P REFCLK_N EVDD12_2 HSOP HSON EGND2 DVDD12_2

VCTRL12 L_TDP L_TDN L_RDP L_RDN MDIP2 MDIN2 MDIP3 MDIN3 FB12 +VDD33 EESK EEDI +VDD33 EEDO EECS +VDD12

L_TDP L_TDN L_RDP L_RDN L_TRDP2 L_TRDM2 L_TRDP3 L_TRDM3

To Transformer

+3VSUS R3315 0Ohm 40 mil +VDD33

C3326 0.1UF/10V C3327 22UF/6.3V C3328 0.1UF/10V C3329 0.1UF/10V GND

071212 change P/N

R3316 0Ohm 40mil +AVDD33

C3330 0.1UF/10V C3331 0.1UF/10V

R3313 0Ohm CLK_LAN_REQ# 29

071120 Reserved

R3311 @ 0Ohm

To SB

21,43,53 PCIE_WAKE#

+EVDD12

Pin.33 is Clkreq# pin similar to Clkrun function in the PCI interface. If this function not implemented, make this pin floating or connect to the ground.

071121 close to LAN CHIP To SB

PCIE_RXN1_LAN_L C3335 0.1UF/10V PCIE_RXP1_LAN_L C3332 0.1UF/10V PCIE_RXN1_LAN 11 PCIE_RXP1_LAN 11

071129 Correct net name

5,12,20,30,43,53,62 BUF_PLT_RST# R3312 0Ohm

From SB

CLK_PCIE_LAN# 29 CLK_PCIE_LAN 29 From Clock Gen.

PCIE_TXN1_LAN 11 PCIE_TXP1_LAN 11

From SB

071217 Base on Design IP

+VDD33 R3303 3.6KOhm

U3302 N/A AT93C46

EECS EESK EEDI EEDO CS SK DI DO VCC DC ORG GND

C3312 @ 0.1UF/10V

25MHz Crystal

XIN_LAN XOUT_LAN X3301 25Mhz C3333 27PF/50V C3334 27PF/50V GND

R3314 0Ohm GND_AGND_A

<Variant Name>

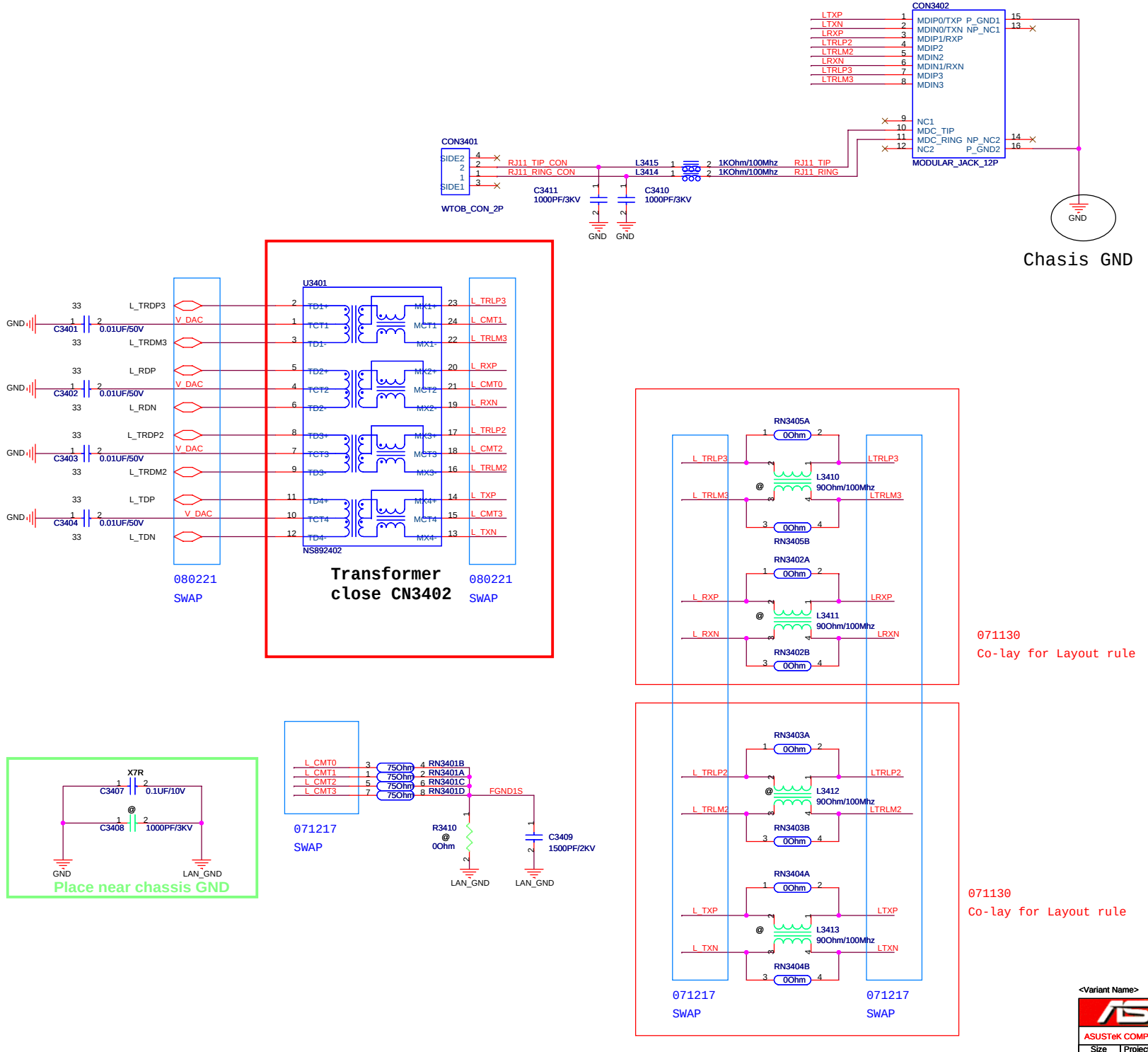
ASUS ASUSTeK COMPUTER INC

Title : LAN-RTL8111C

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

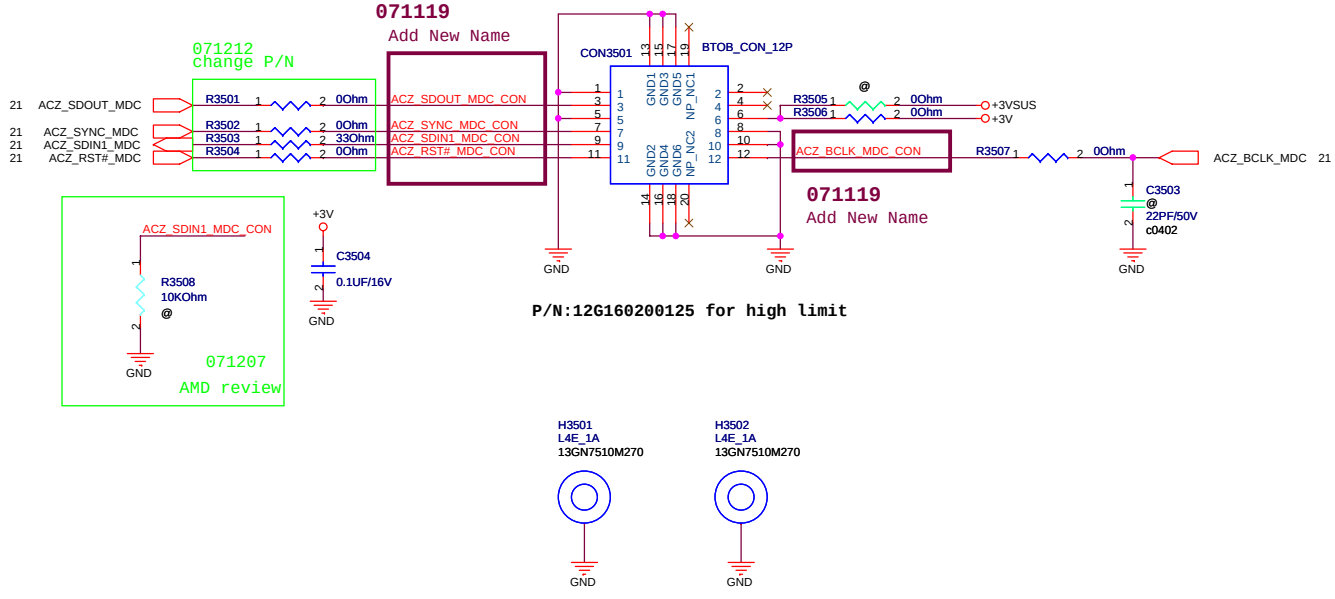
Date: Monday, May 19, 2008 Sheet 33 of 94



<Variant Name>

ASUSTeK COMPUTER INC	Title : LAN-RJ45	
	Engineer: Richard Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 34 of 94	

MDC



<Variant Name>

ASUSTeK COMPUTER INC	Title : LAN-MDC	
	Engineer: Richard Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 35 of 94	

ALC663		
	Mount	R3614,R3674,R3675,RX3612,RX3613,R3618,R3613,R3612,C3629,C3608
	NO Mount	R3672,R3673,R3631,R3632,R3608

AUDIO POWER

CODEC:ALC662 / ALC663

Mount R3614 For ALC663 ;
Mount R3617 For ALC662

Need to Check

Digital

FROM ICH

Mout For ALC663

For ALC663
Need to Check

Mout C3629 For ALC663

Reserved For ALC663;
NC For ALC662

Cap-less with pop-noise, RX3612, R3X613 mount 0 Ohm, mount R3777,R3778 no mount CE3751,CE3752,R3758,R3759, R3756, R3757

Isolate the voltage level

Mout R3674 and R3676 For ALC663 ;
Mount R3673 and R3672 For ALC662;

07116

Unuse in F5Z

Unuse in F5Z

080519

U3603 MAX8863 / MAX8863TEUK

Vout=1.25*(1+(100K/34.8K))=4.84V
Vdrop about 150mV@100mA
2nd source:GMT G923 470T1UF SOT23-5
(P/N:06G007342012)

FOR NORMAL FUNCTION .

Mount RX3613 and RX3612 For ALC663;
Mount R3632 and R3631 For ALC632;

TO HP

TO INTERNAL MIC

TO EXTERNAL MIC

TO SPK AMP

THE VALUE DEPEND ON C3635/C3636 TO MEET THE RECOMMENDATION VALUE(0.47UF).

07116

Del Audio DJ Function

071207
AMD review

DETECTION

EXT MIC DETECT.

Mount R3618 For ALC663 ;
Mount R3608 For ALC662;

FOR HP DETECT.

For ALC663 Cap-less detect pin

PC BEEP

Reserve for Cardbus controllor that has PCMCIA function.

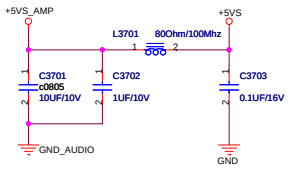
IF NO PCMCIA,DNI IT.

FROM ICH

For EMI

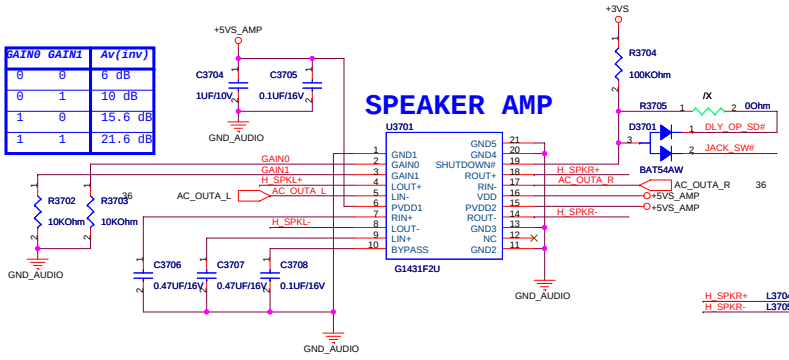
<Variant Name>			
ASUSTeK COMPUTER INC	Title : CODEC-ALC662		
	Engineer: Richard Lu		
Size C	Project Name F7Z		Rev 1.0
Date: Monday, May 19, 2008	Sheet 36 of 94		

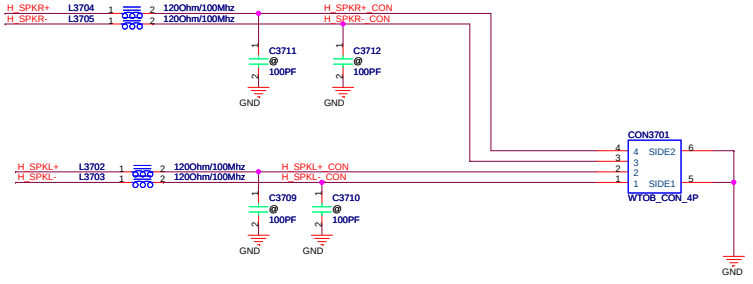
AMP POWER



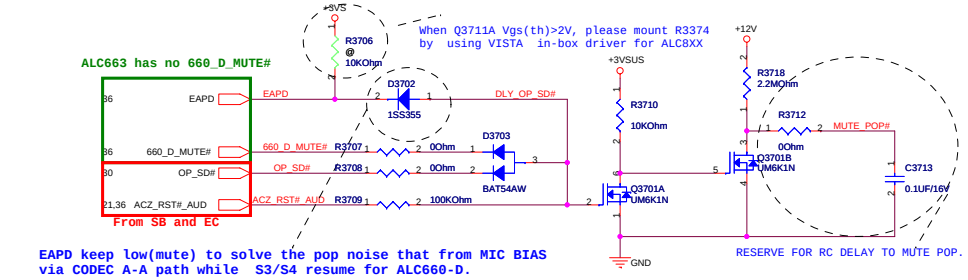
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

SPEAKER AMP



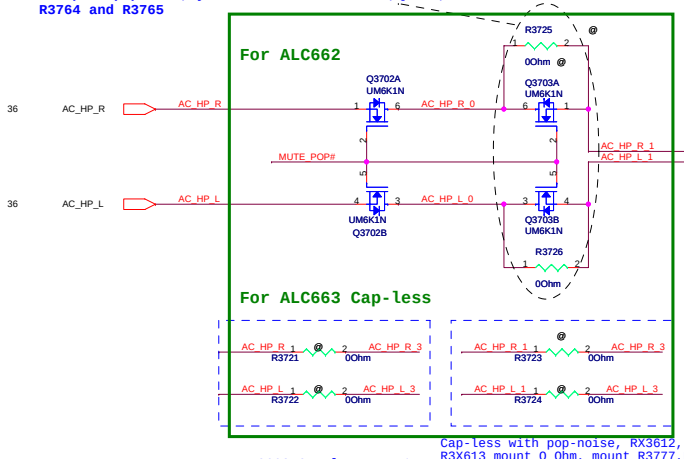


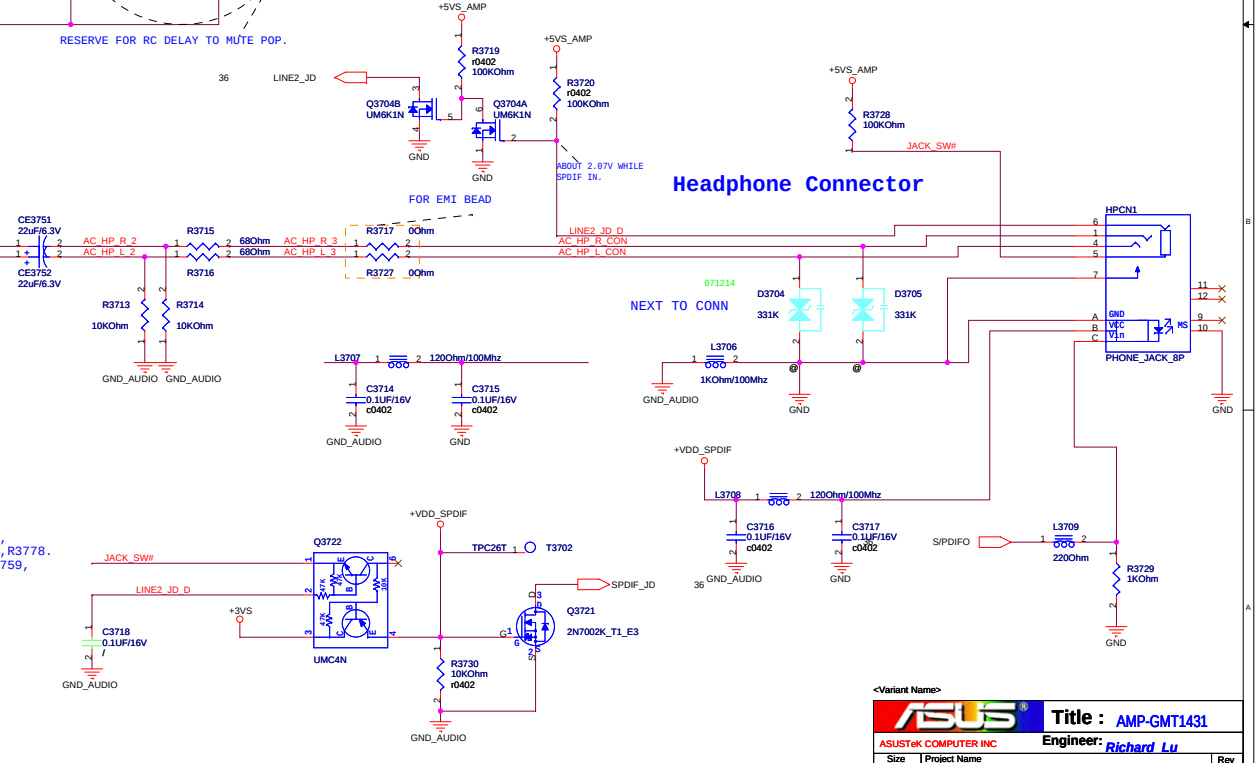
MUTE CONTROL



TYPE	LINE_OUT	S/PDIF_OUT	NC
LINE2_JD_D	L	H	H
JACK_SW#	L	L	H

EAPD keep low(mute) to solve the pop noise that from MIC BIAS via CODEC A-A path while S3/S4 resume for ALC660-D.
Base on pop noise by each model.if your model do not care the A-A path pop-nose, you can not mount D3711,Q3755,but mount R3764 and R3765

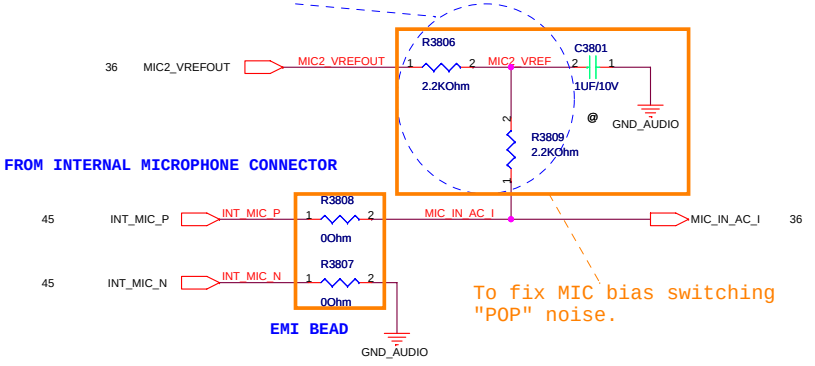




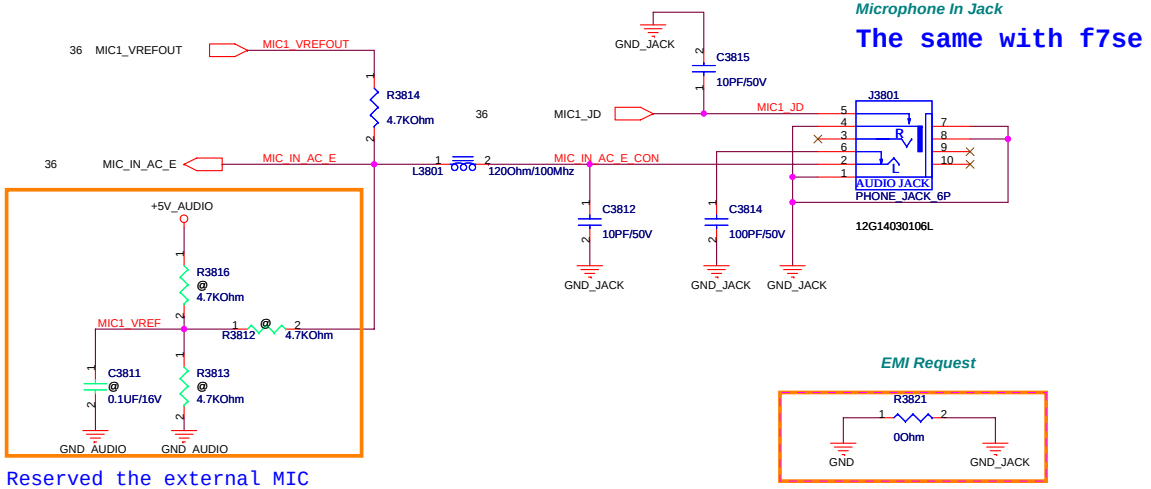
071116 Change form F5R to Design IP

INTERNAL MICROPHONE

If EAPD available(fix MIC bias switching "POP" noise):
Replace R3801,R3802 by one 4.7K ohm resistor.
DNI C3801.



EXTERNAL MICROPHONE

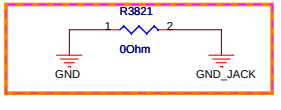


Reserved the external MIC bias(T filter).

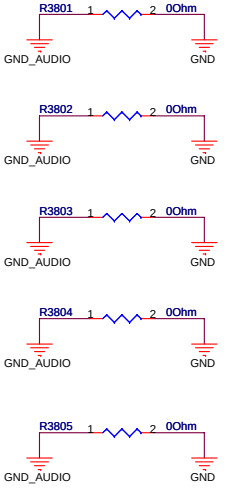
Microphone In Jack

The same with f7se

EMI Request

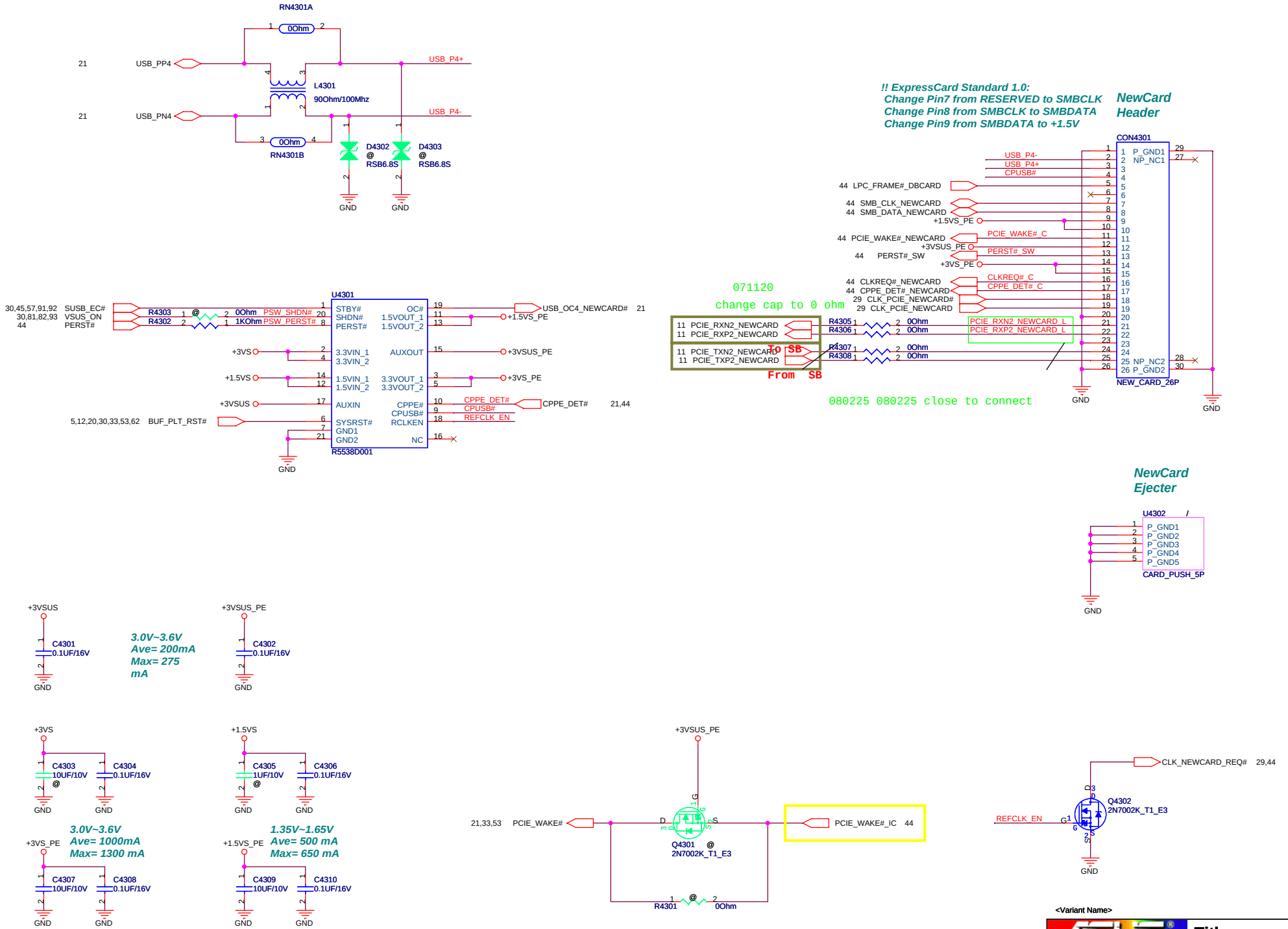


F7Z 071212 change 0 ohm P/N



<Variant Name>

ASUSTeK COMPUTER INC	Title : MIC-IN Jack	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 38 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

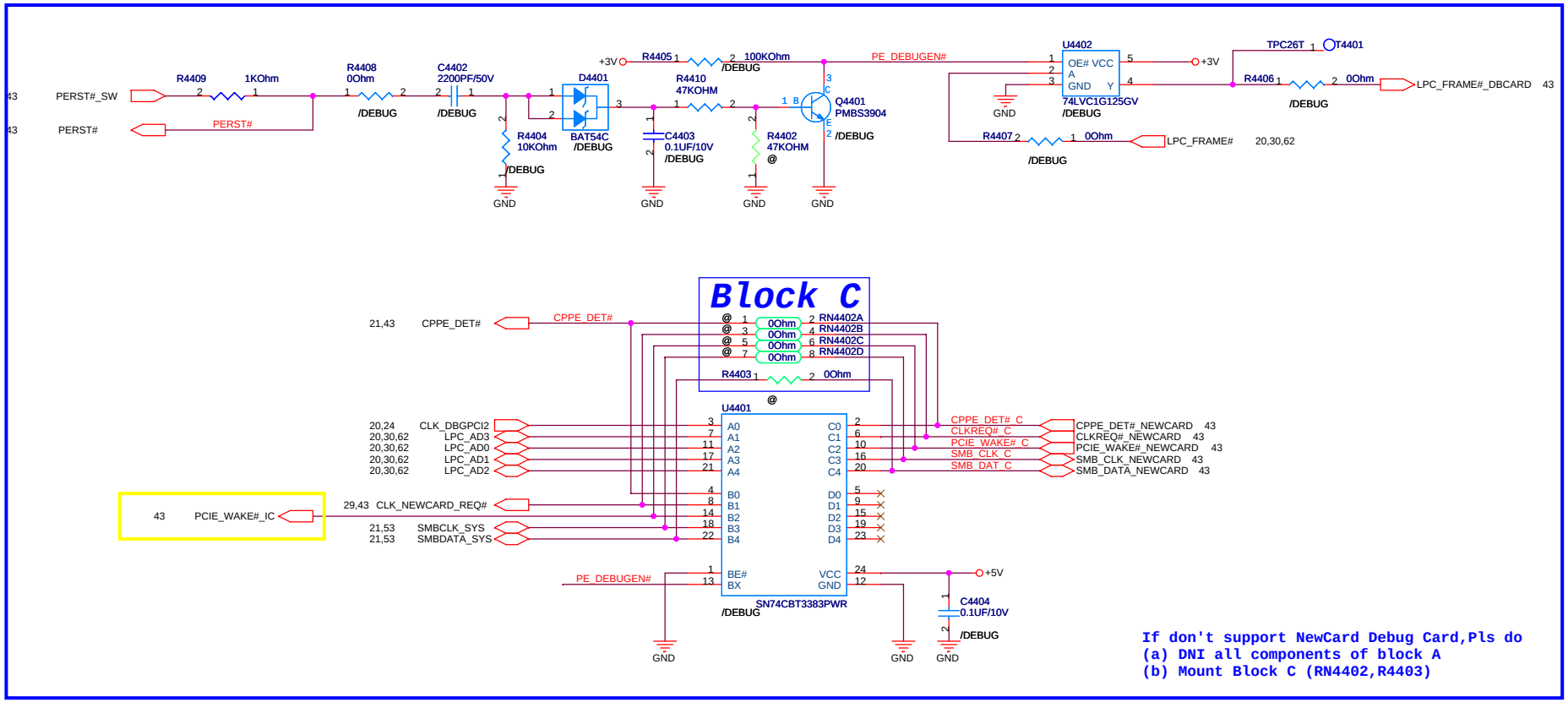
Title : NEWCARD

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

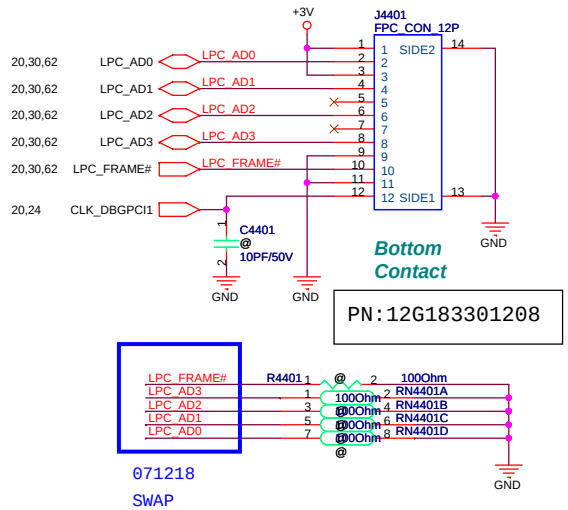
Date: Monday, May 19, 2008 Sheet 43 of 94

Block A



For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.

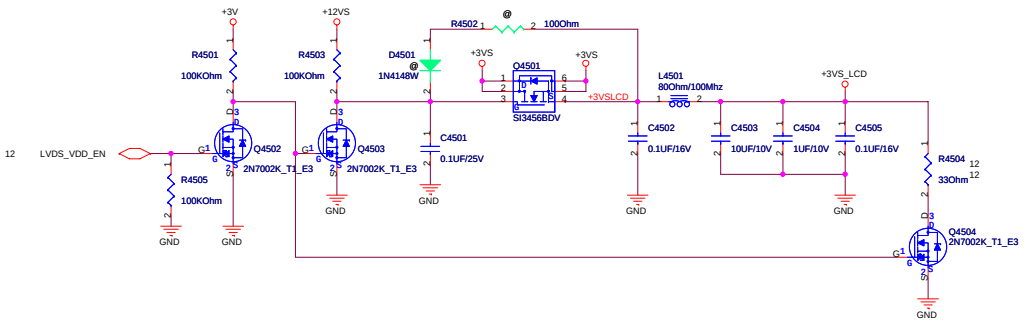


<Variant Name>

ASUSTeK COMPUTER INC	Title : DEBUG	Engineer: Richard_Lu
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 44 of 94	

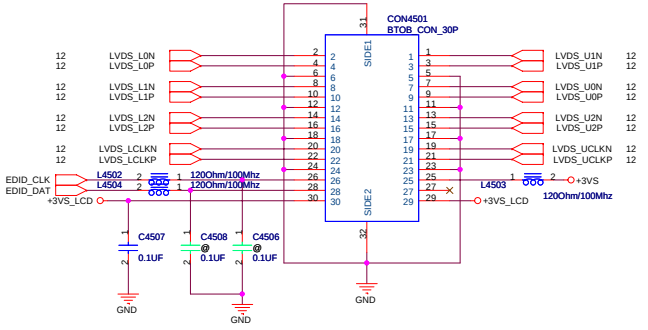
LCD Backlight Control

LCD Power



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface

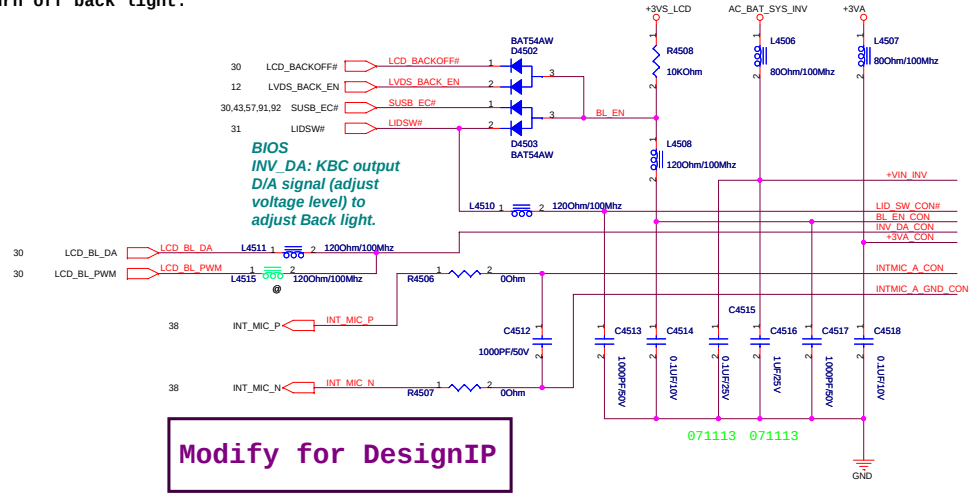


INVERTER Interface

Delete LID_SW SCH

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

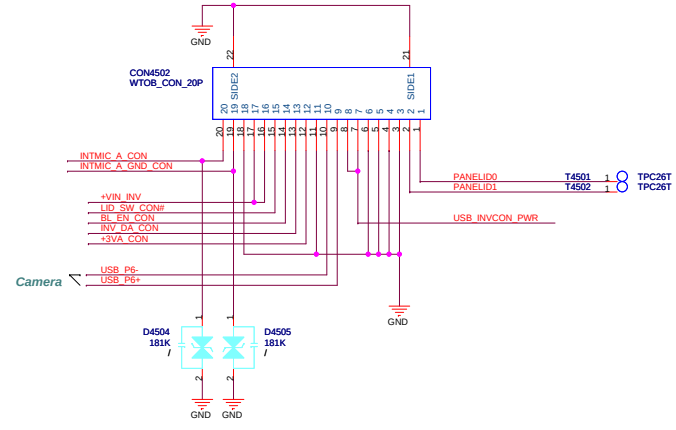
connect to JP8805
071203



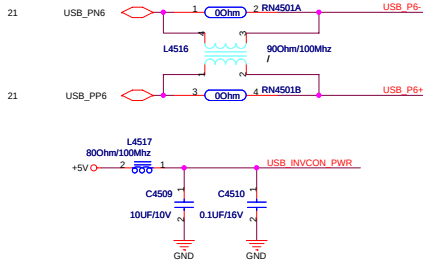
BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

Modify for DesignIP

INVERTER
Interface/Speaker CONN.

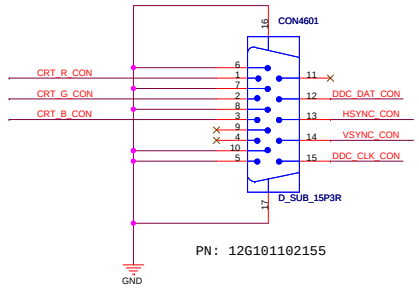


EMI REQUEST

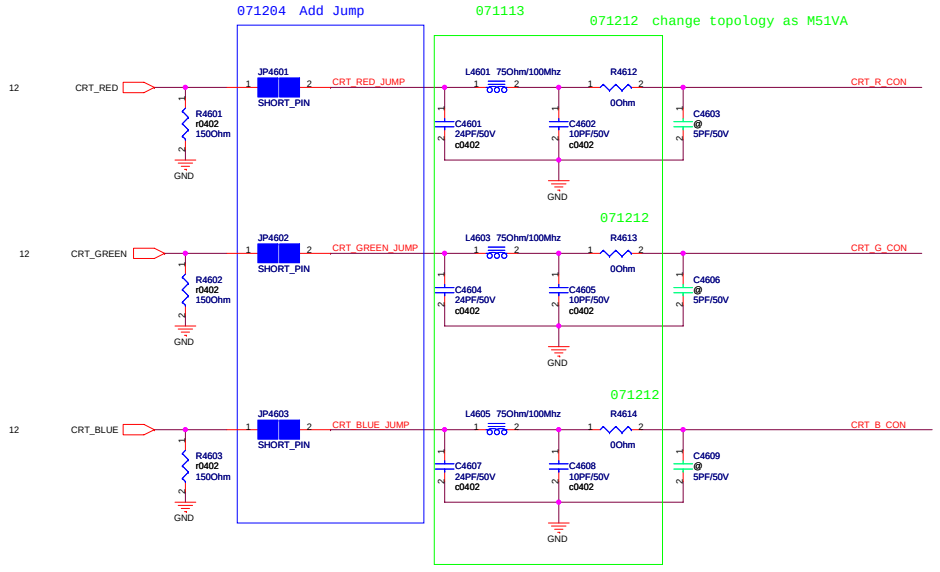


<Variant Name>

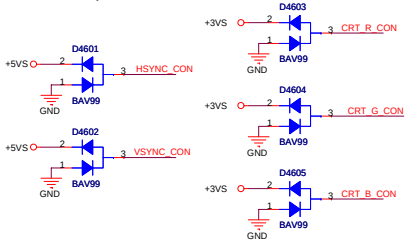
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Richard_Lu	
Size: C	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 45 of 94	

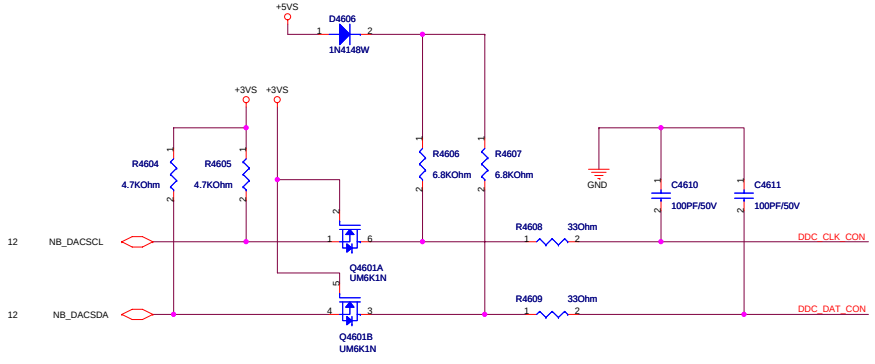


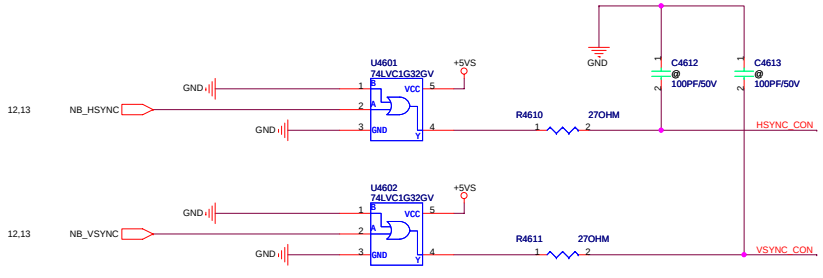
PN: 12G101102155



PLACE ESD Diodes near VGA port



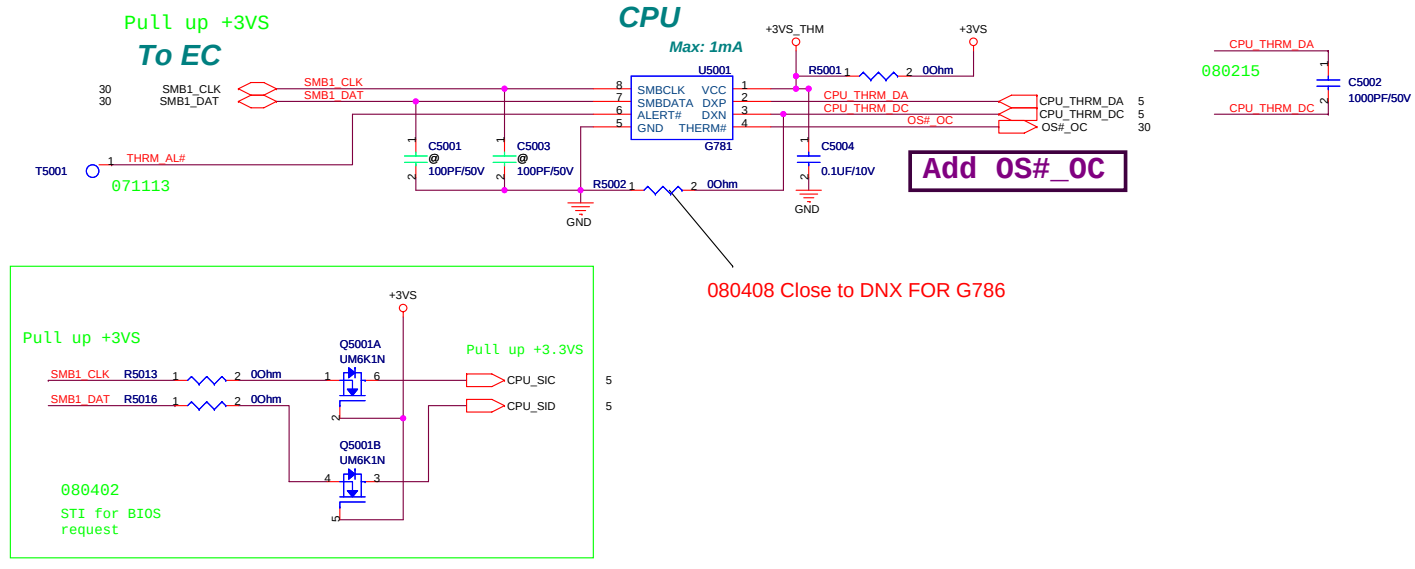




<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT	Engineer: Richard Lu
Size: C	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 46 of 94	

Thermal Sensor

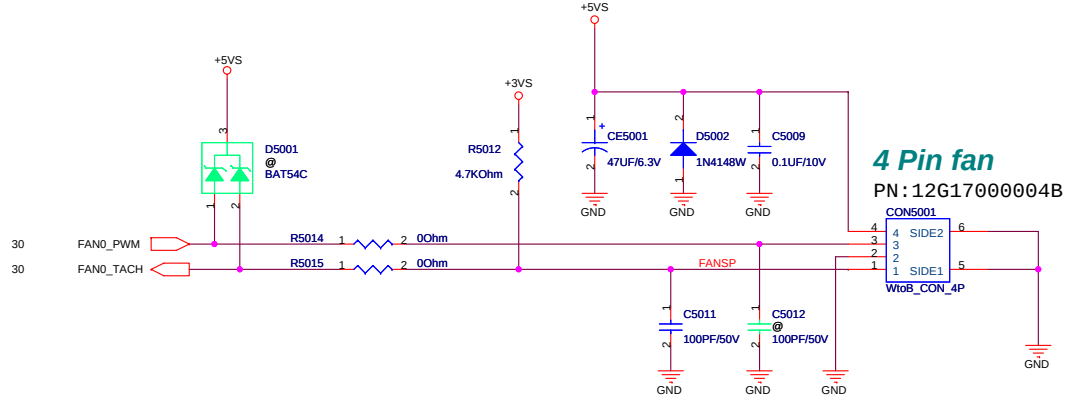


Route H_THERMDA and H_THERMDC
on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

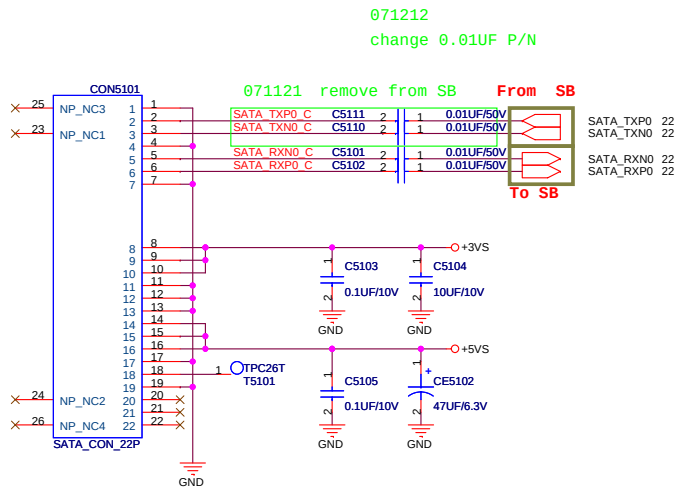
DC FAN Control



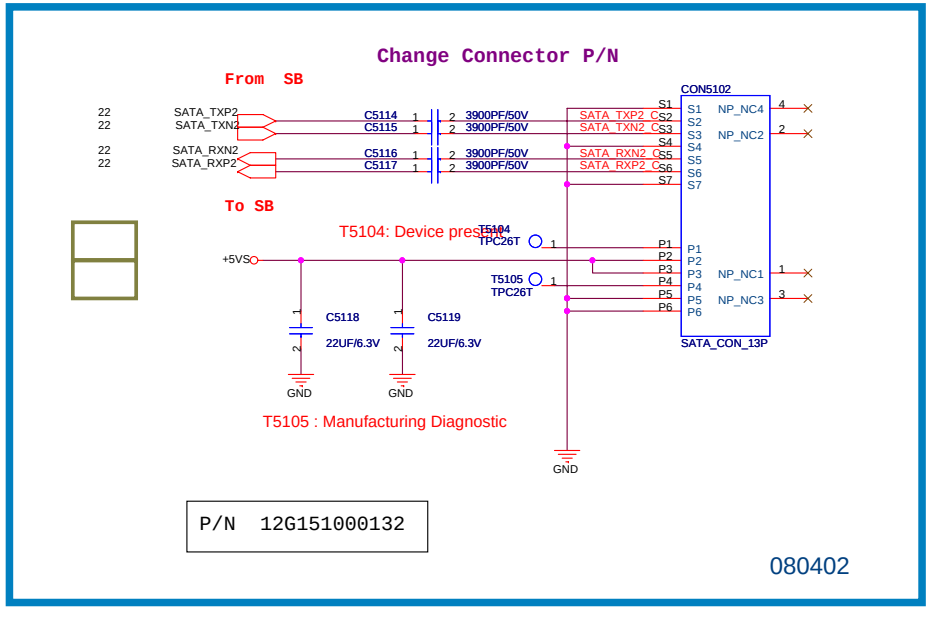
<Variant Name>

ASUS	Title : THER SENSOR & FAN	
ASUSTeK COMPUTER INC	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 50 of 94	

SATA HDD



ODD

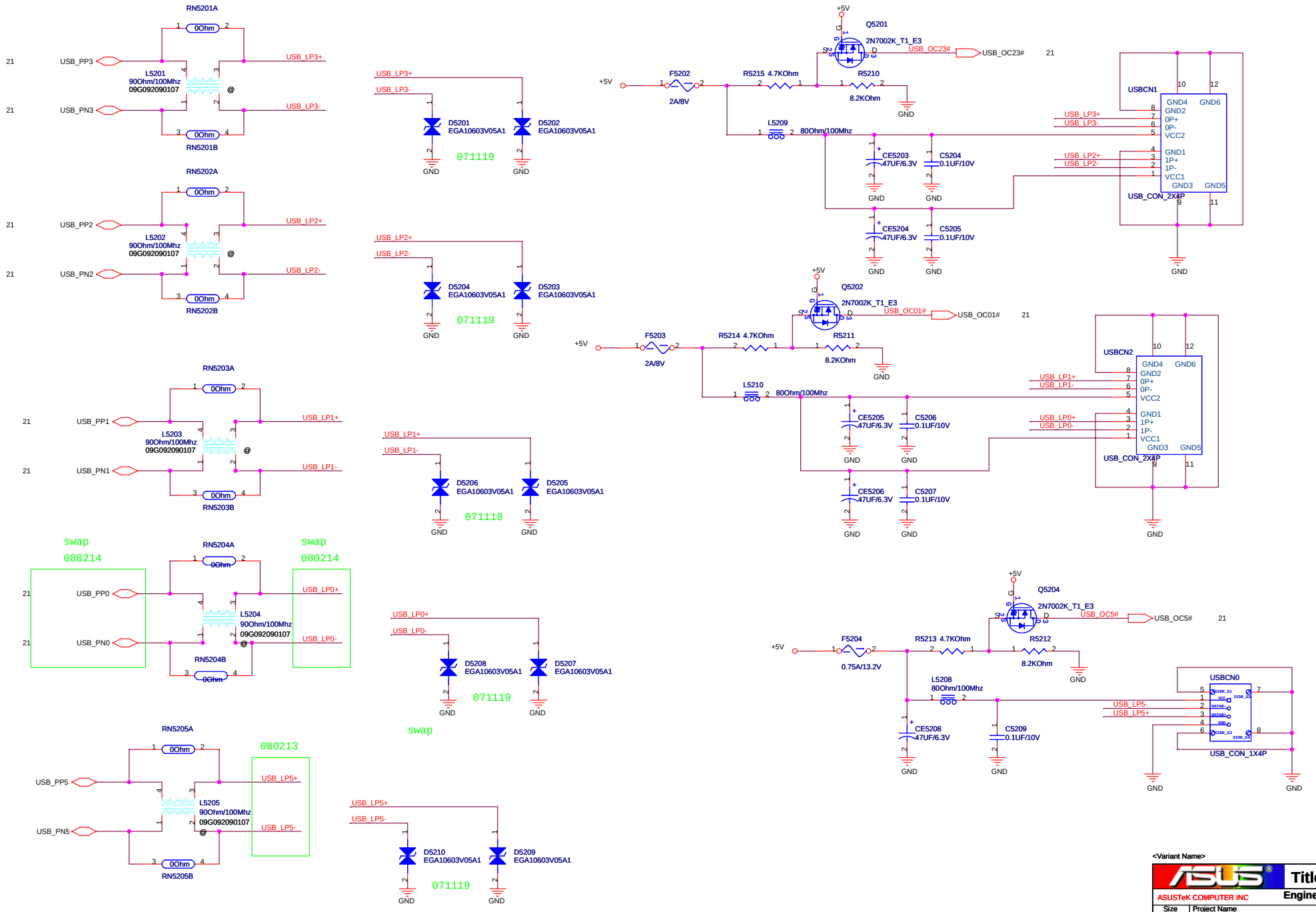


<Variant Name>

ASUS	Title : HDD & CD-ROM		
ASUSTeK COMPUTER INC	Engineer: Richard_Lu		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 51 of 94		

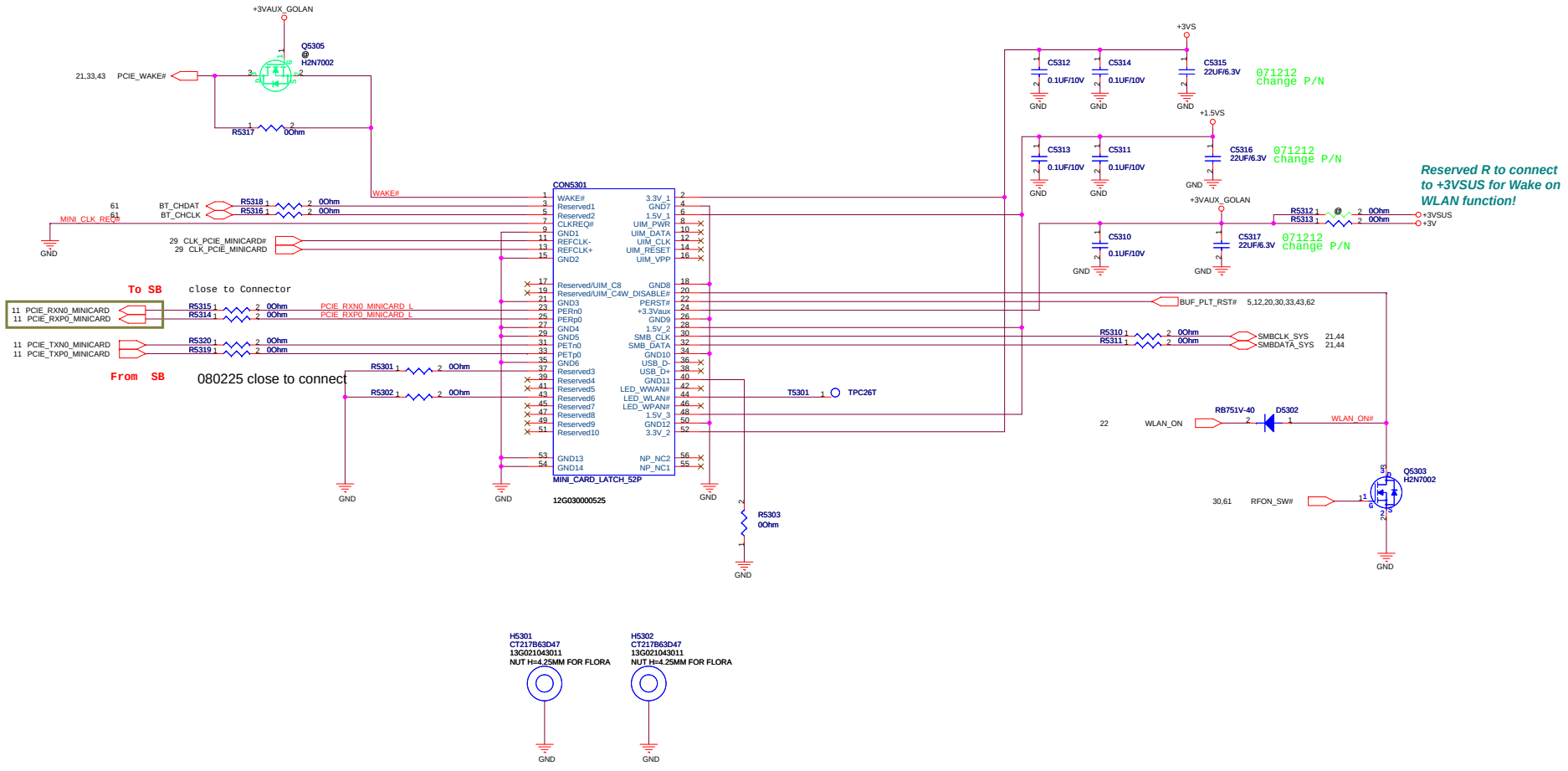
071119 change common choke and R P/N

Change all MOS with ESD part



<Variant Name>

ASUSTeK COMPUTER INC	Title : USB CONN	Engineer: Richard_Lu
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 52 of 94	



<Variant Name>

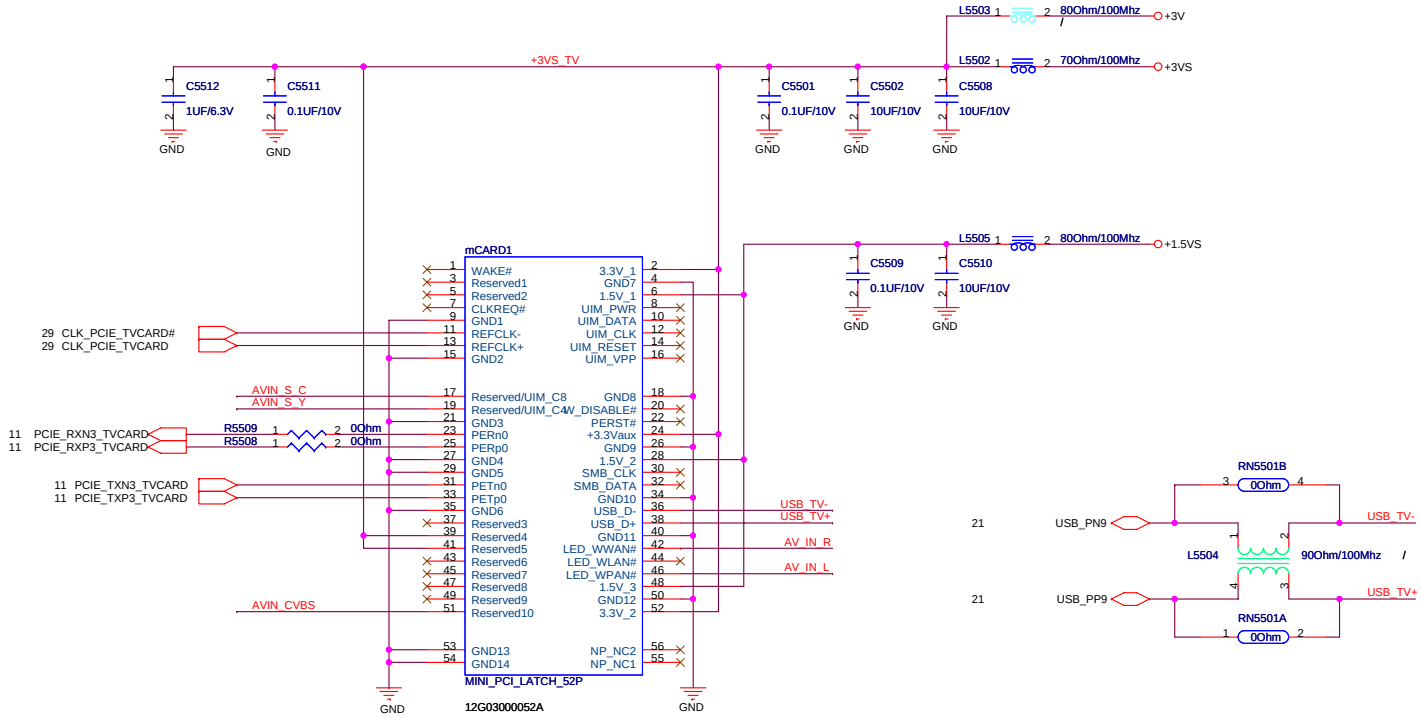
ASUSTeK COMPUTER INC

Title : MINICARD

Engineer: Richard Lu

Size	Project Name	Rev
C	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 53 of 94

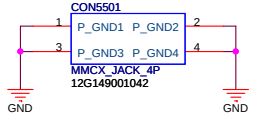


H = 5.2mm

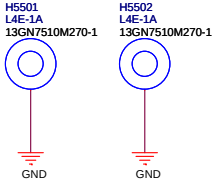
FOR TV TUNER

(UWB OPTION)

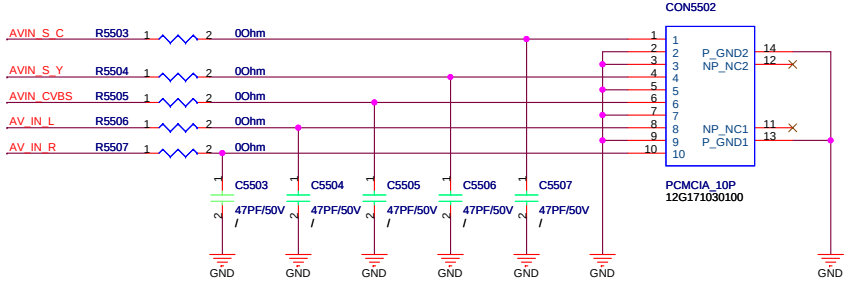
TV Conn.



ME P/N : 14G152075000



H = 3.0mm

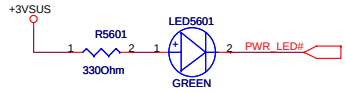


<Variant Name>

ASUS	Title : *	
ASUSTeK COMPUTER INC	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 55 of 94	

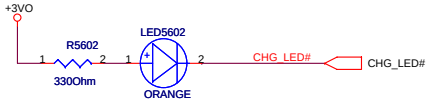
LED

For POWER LED



PWR_LED# 30

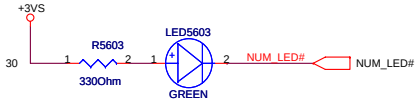
BATTERY LED



CHG_LED#

Num Lock

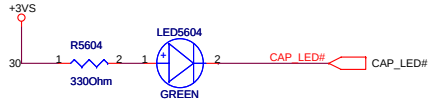
071122



30 NUM_LED#

Cap Lock

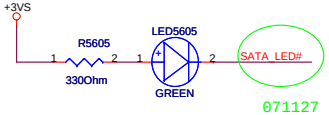
071122



30 CAP_LED# 30

SATA/IDE LED

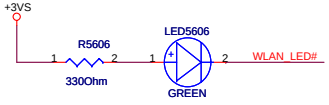
071122



071127

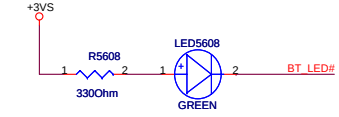
WireLess LED

071122



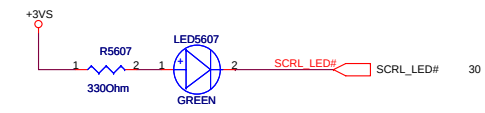
BT LED

071122



Scroll Lock

071122

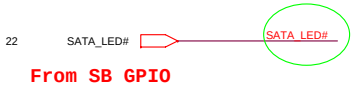


30 SCRL_LED# 30

Change all LED for 5mA

delete D5601

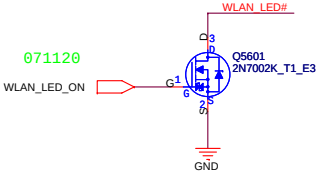
071127



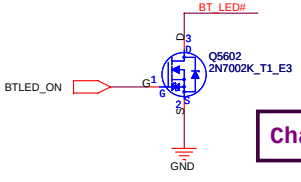
22 SATA_LED#

From SB GPIO

071120



22 WLAN_LED_ON



22 BTLED_ON

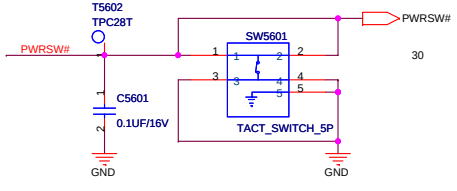
Change all MOS with ESD part

F5Z SWITCH CIRCUIT

Move SW from P32 to P56

Add SHUT Down SCH

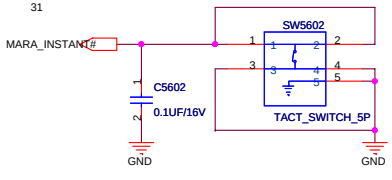
Power SW.



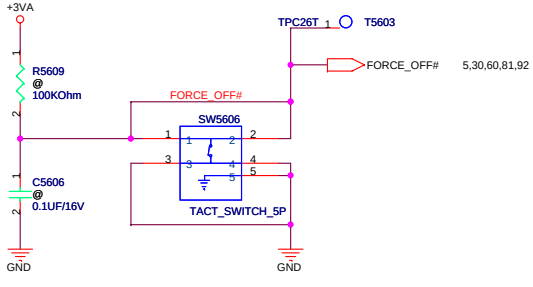
30 PWRSW# 31

P/N: 12G091030050

Marathon SW.



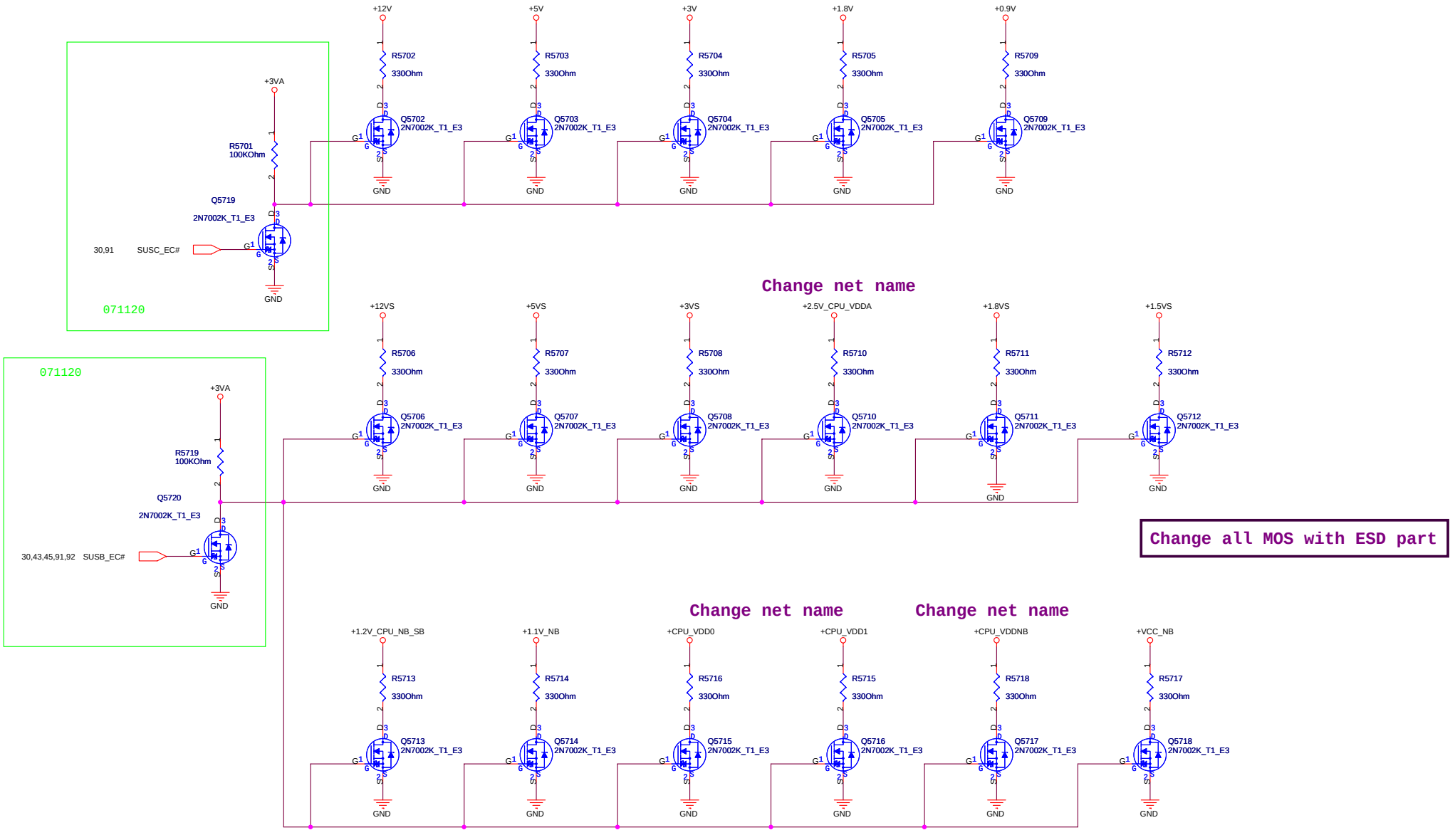
SHUT_DOWN#



FORCE_OFF# 5,30,60,81,92

<Variant Name>

ASUSTeK COMPUTER INC	Title : LED/PWR SWICH	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 56 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

Title : DISCHARGE CKT

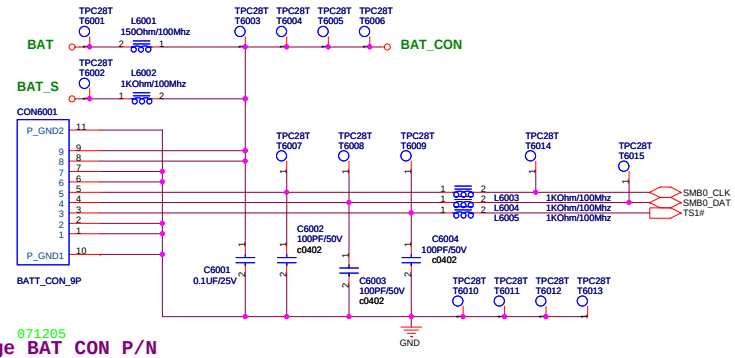
Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 57 of 94

BATTERY

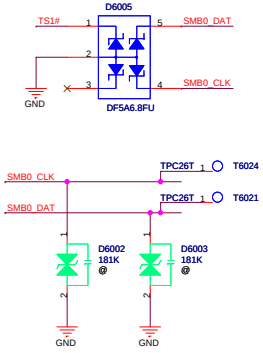
071120 cahnge PL->L,PT->T,PC->C



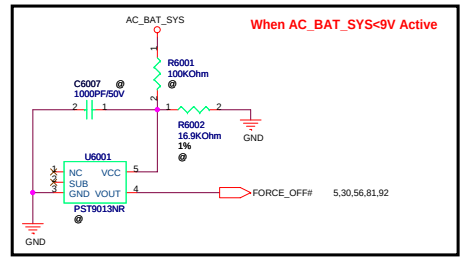
071205
Change BAT CON P/N

Reference To M51

071203 change footprint



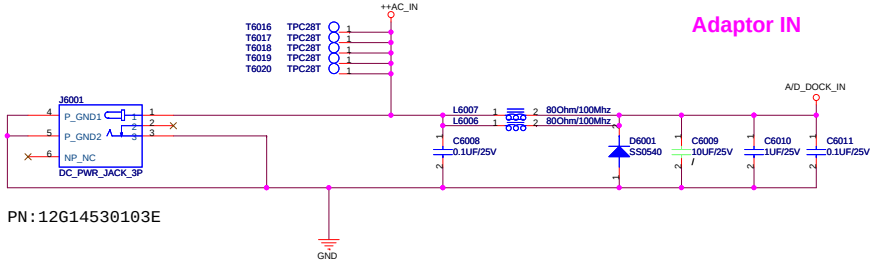
Without Battery & Pull out Adapter



Add for AC Adapter protect

DC JACK-IN

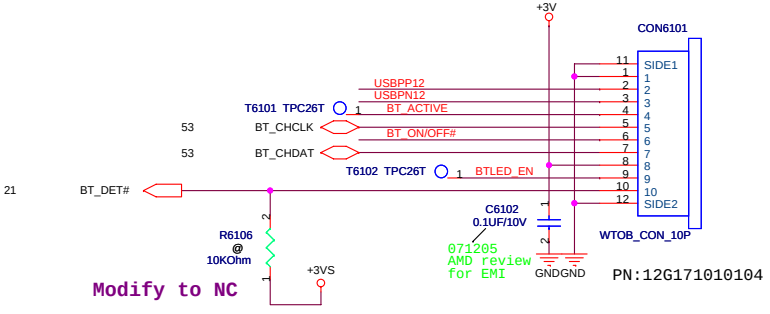
Adaptor IN



PN:12G14530103E

071218
Delete GND_DC , Bead
,and Test Point

For Bluetooth



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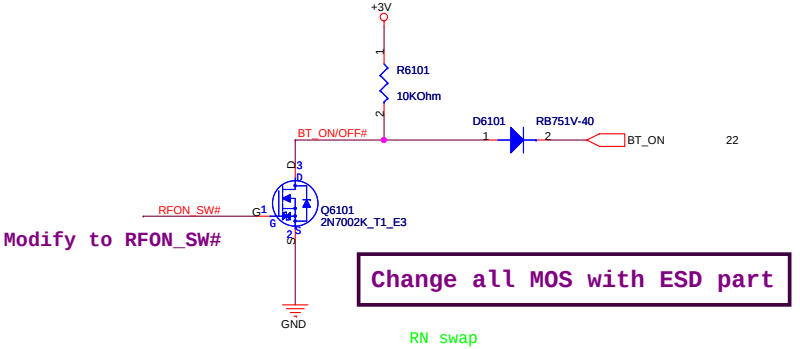
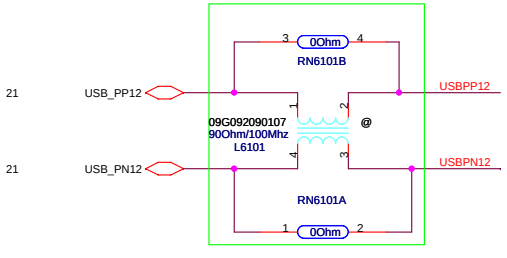


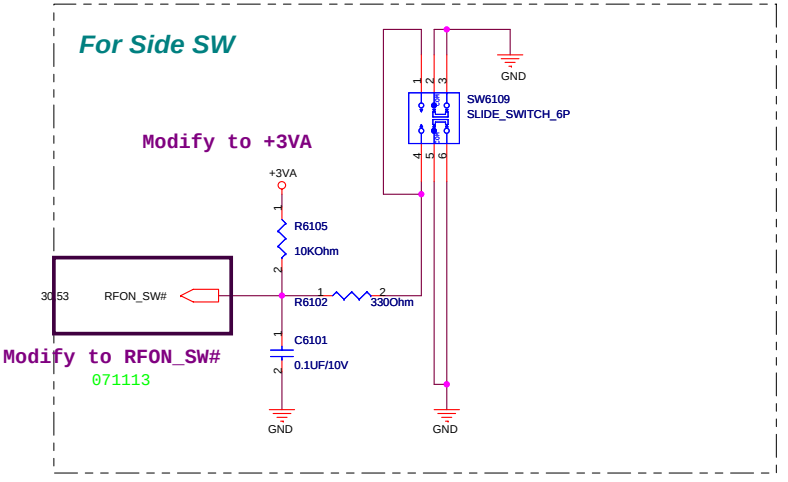
Change all MOS with ESD part

RN swap
071214



071120 change common choke and R P/N

For Side SW

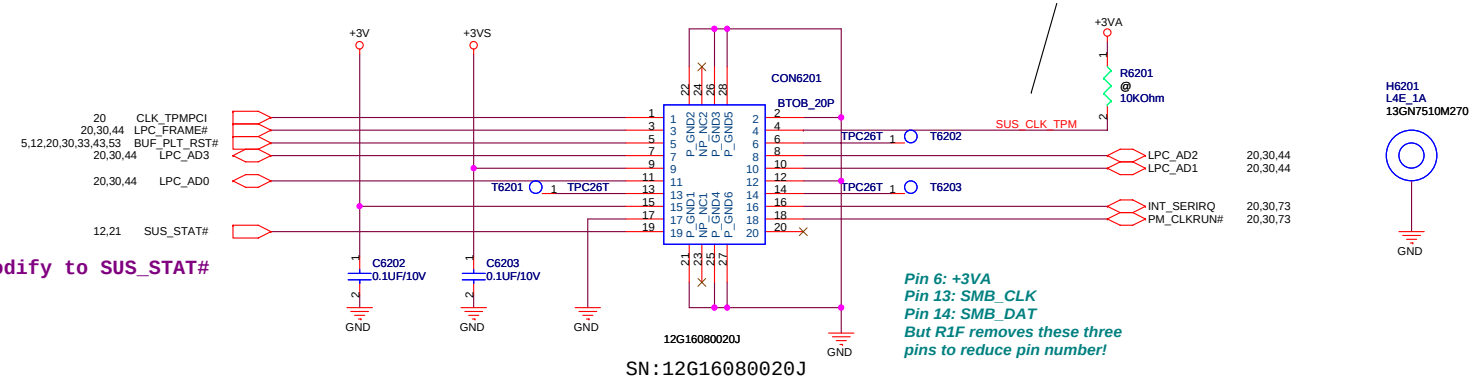


<Variant Name>

ASUS	Title : BT & Slide SW	
ASUSTeK COMPUTER INC	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 61 of 94	

For TPM Module

071120
TPM module has internal crystal



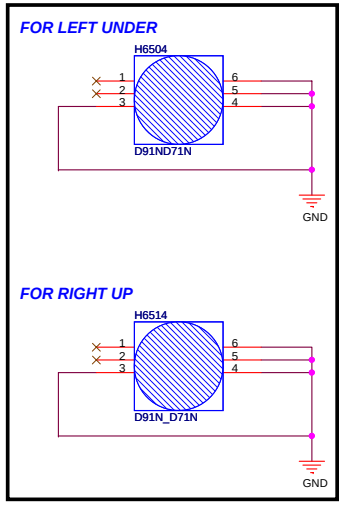
Modify to SUS_STAT#

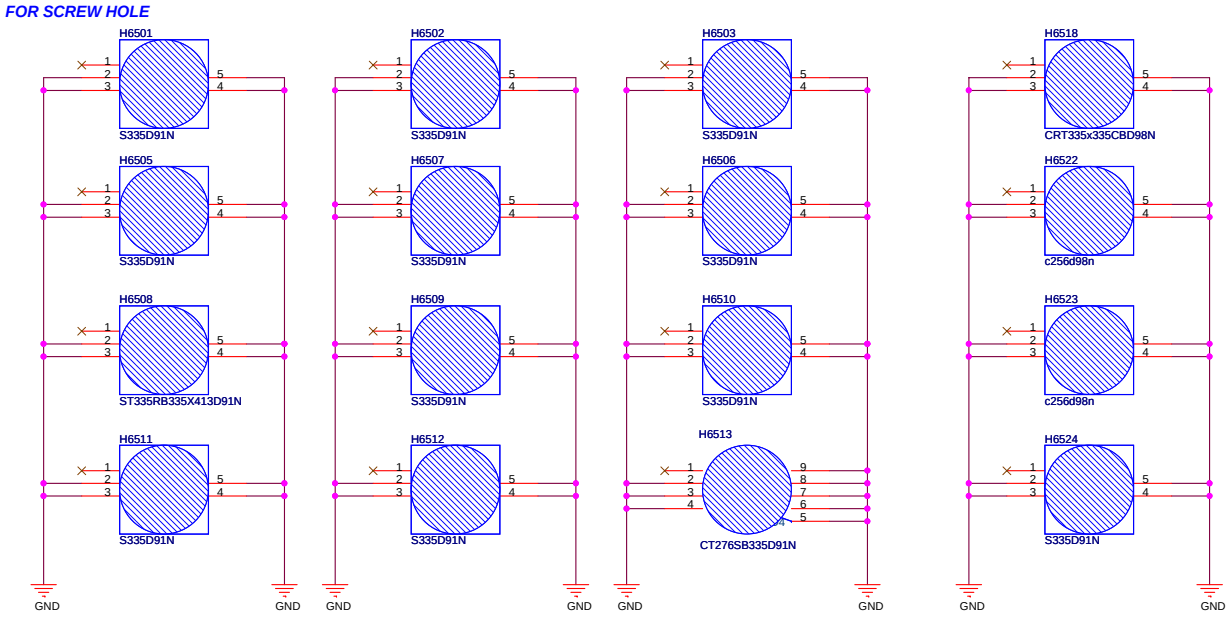
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

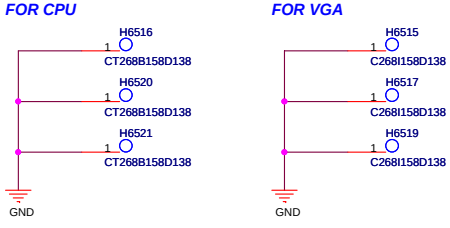
SN:12G16080020J

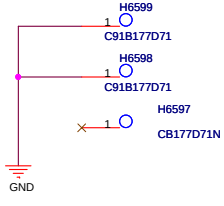
<Variant Name>

ASUS	Title : TPM		
ASUSTeK COMPUTER INC	Engineer: Richard_Lu		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 62 of 94		





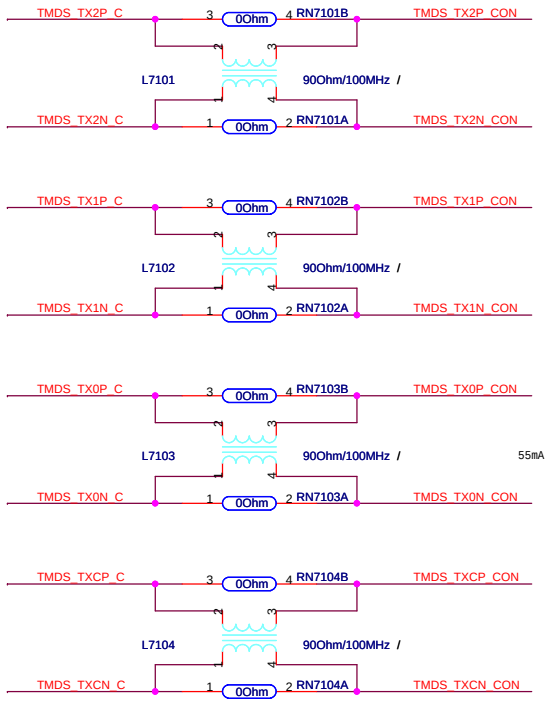


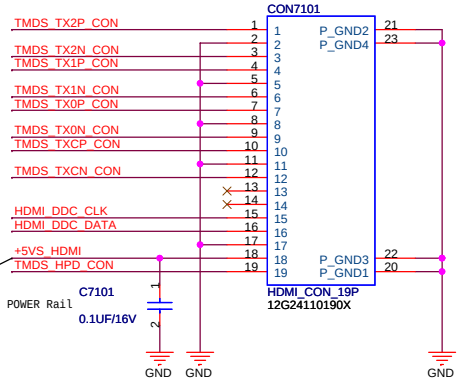


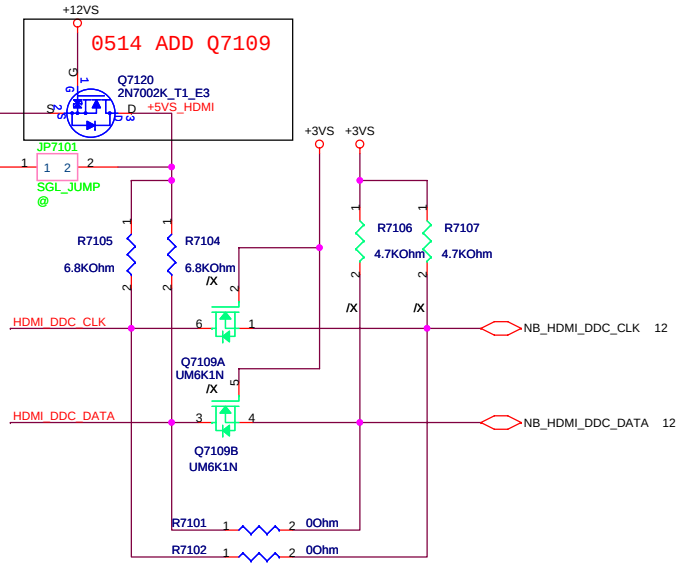
<Variant Name>

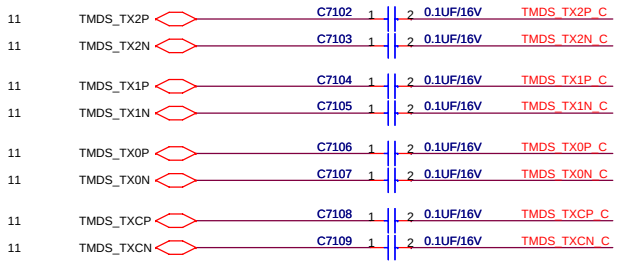
ASUS	Title : Screw Hole	
ASUSTeK COMPUTER INC	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 65 of 94	

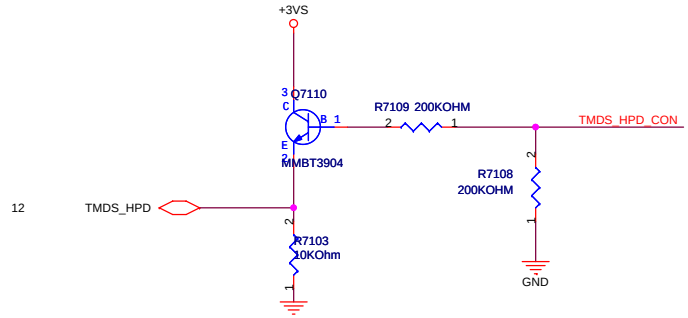
HDMI

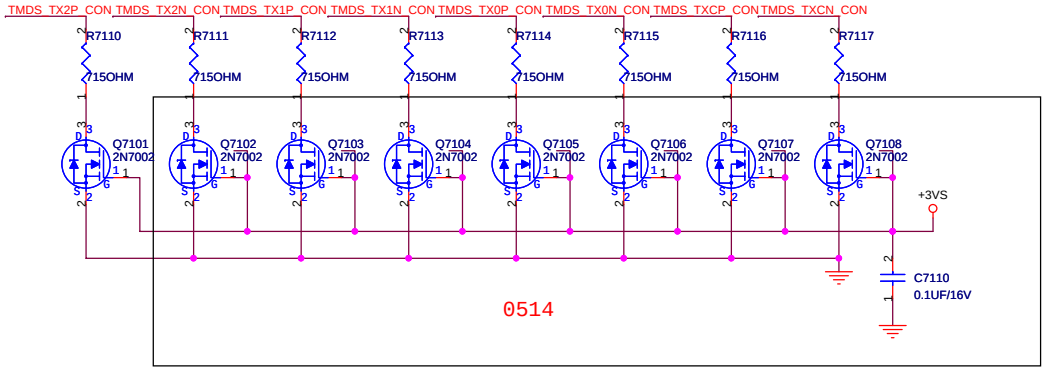






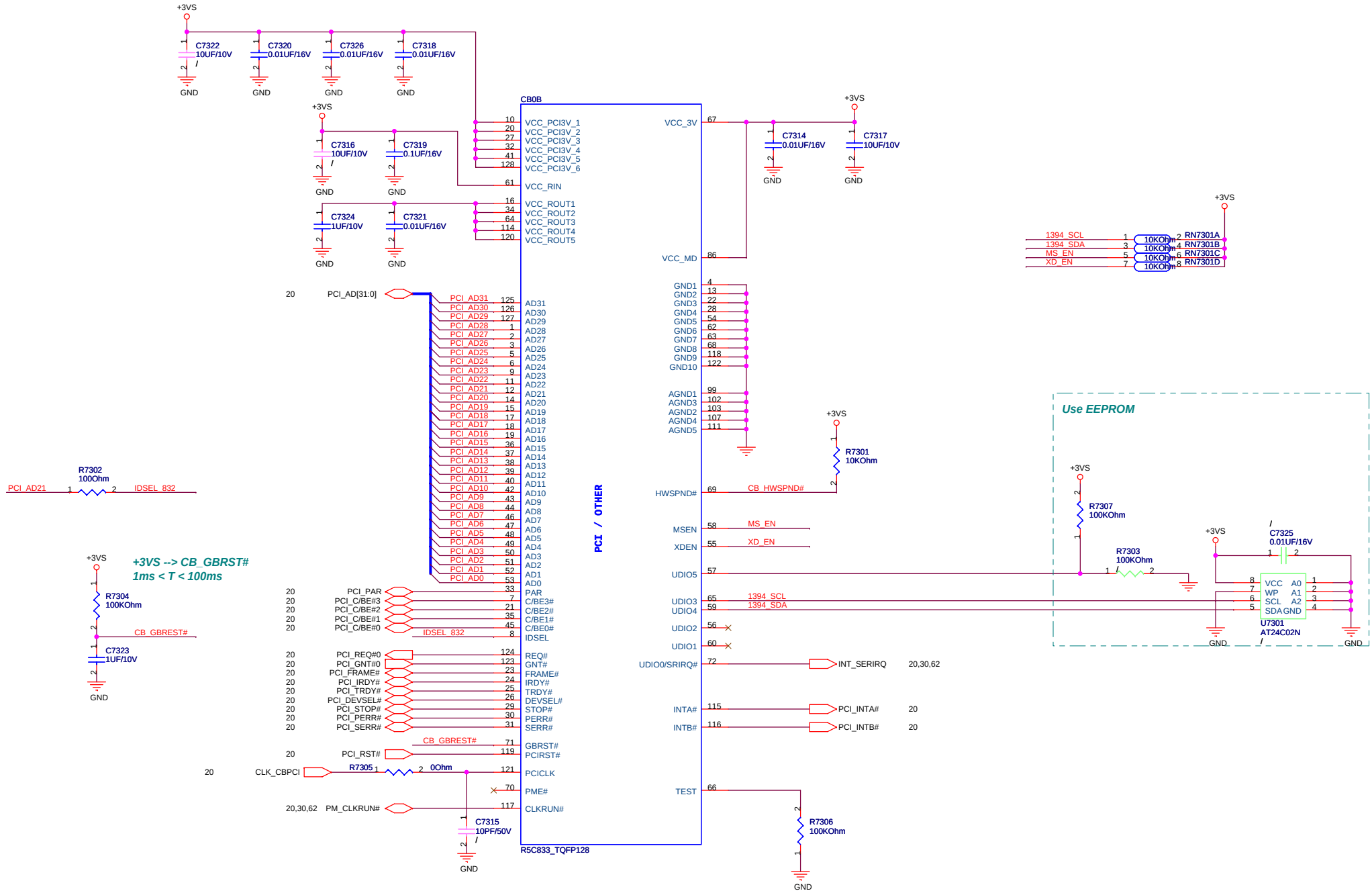






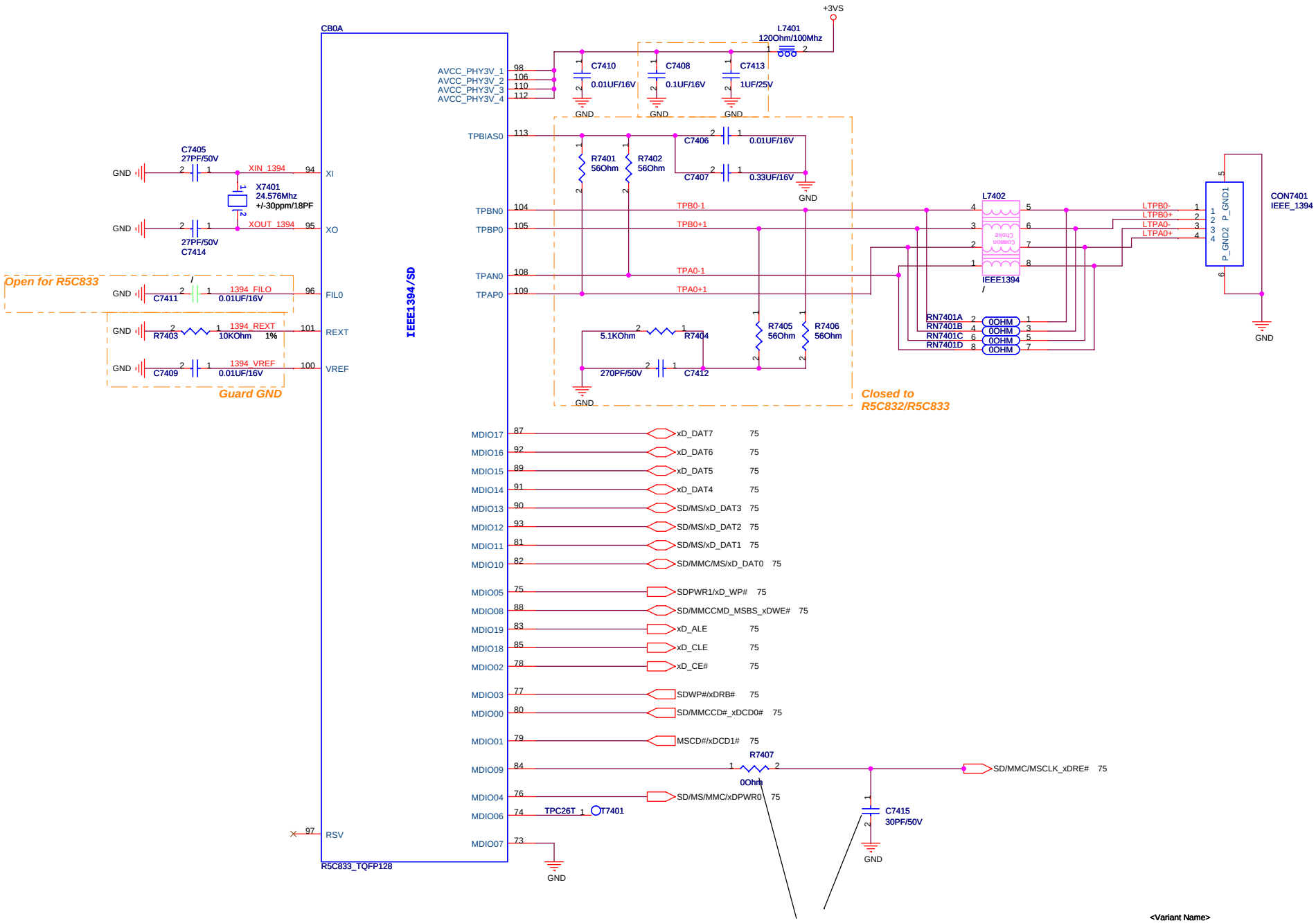
<Variant Name>

ASUSTeK COMPUTER INC	Title : HDMI CON	
	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 71 of 94	



<Variant Name>

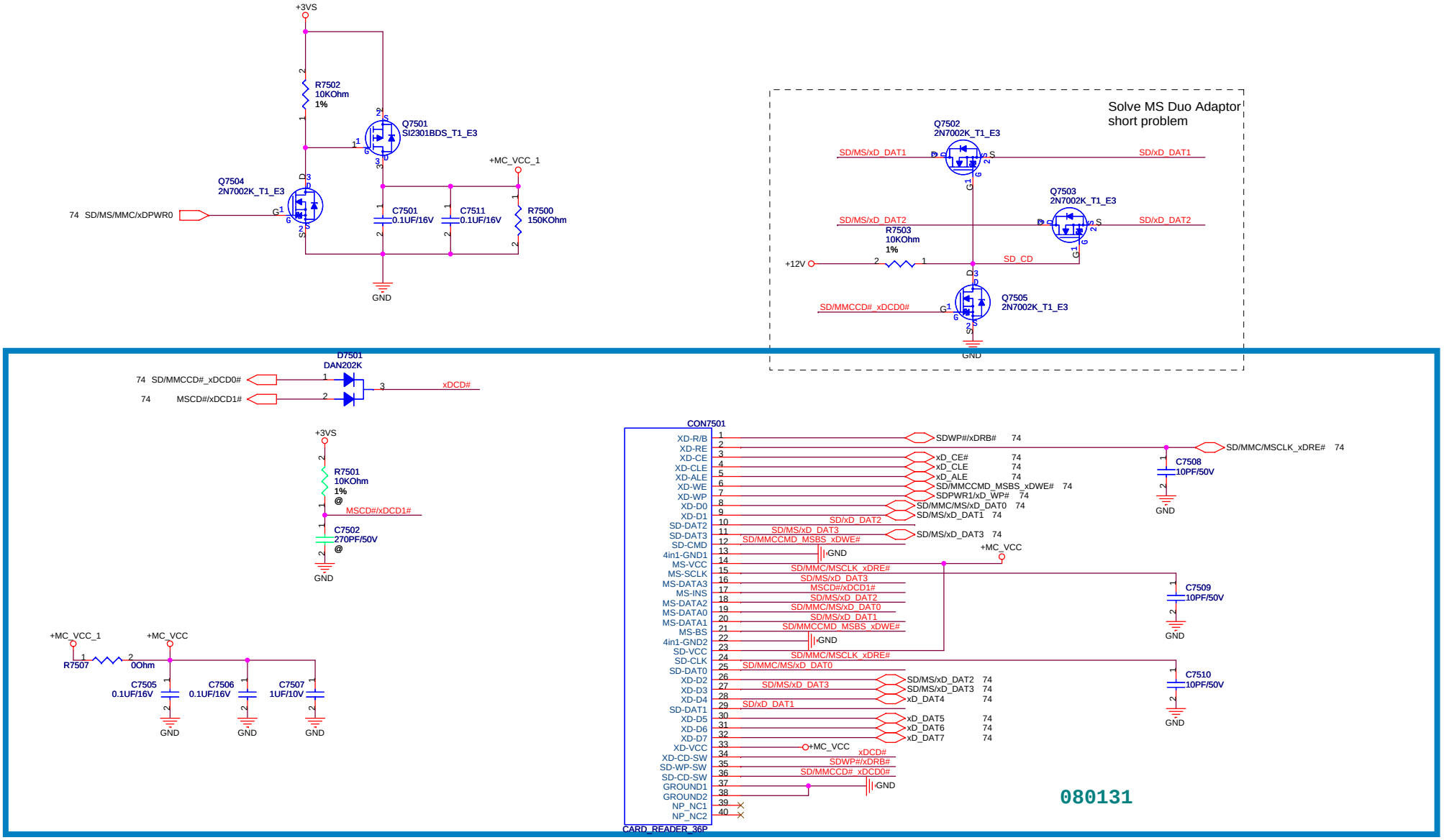
ASUSTeK COMPUTER INC	Title : *	Engineer:
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 73 of 94	



080408 Add r7407 and c7415 for EMI

<Variant Name>

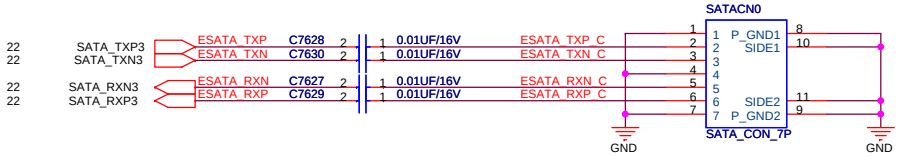
ASUS	Title : *	
ASUSTeK COMPUTER INC	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 74 of 94	



<Variant Name>

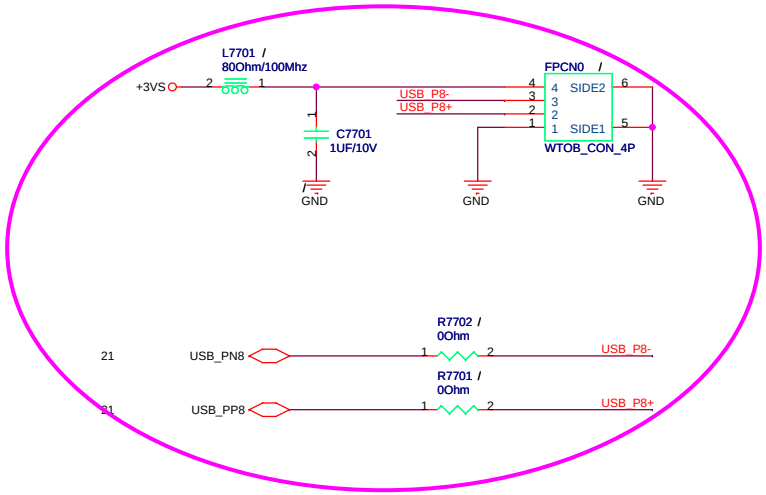
ASUSTeK COMPUTER INC	Title : *	Engineer:
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 75 of 94	

eSATA Connector



<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 76 of 94	



<Variant Name>

ASUS	Title : *	
ASUSTeK COMPUTER INC	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 77 of 94	

080131 Change cardreader connect to 12G340003601.change CDROM connect to 12G151000132 .
080215 1.change thermal sensor to G781,change C5002 to 1000pf
2.fix stuff TMP module can not boot

080217 change C3711/C3712/C3709/C3710 connect to GND
change D7101 to 2 Pin
080219 Remove R3052 and R3108,move D3103 to R3052(N connect to EC side)
change Q9101/Q9107 to 07G005161020(07G005357011)

080221 change ec to 8512 Page82 Page83

080222 add C0651/C0652/C0653/C0654

080225 add R1408/R4307/R4308/R5319/R5320

080408 Add r7407 and c7415 for EMI

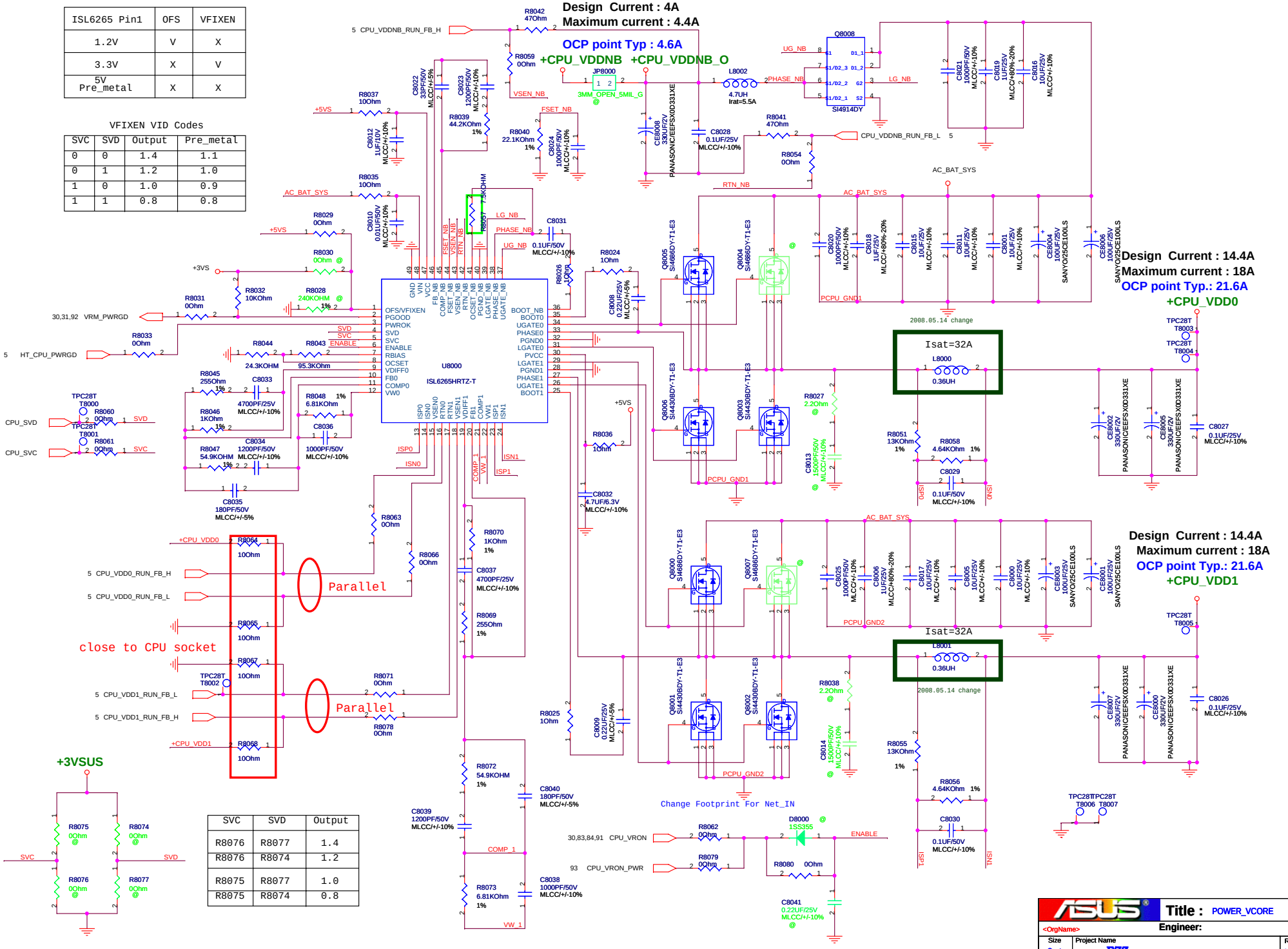
<Variant Name>

ASUS	Title : *	
ASUSTeK COMPUTER INC	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 78 of 94	

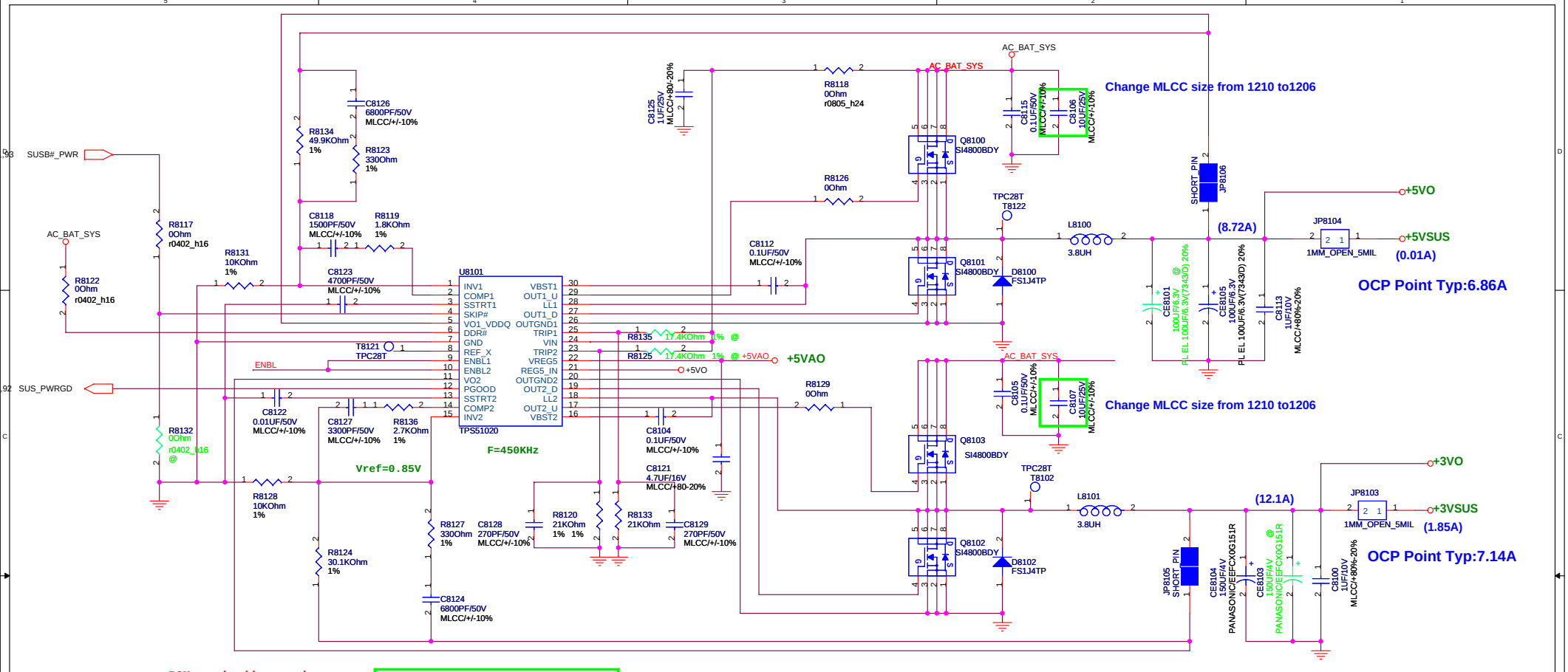
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V Pre_metal	X	X

VFIXEN VID Codes

SVC	SVD	Output	Pre_metal
0	0	1.4	1.1
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.8	0.8



SVC	SVD	Output
R8076	R8077	1.4
R8076	R8074	1.2
R8075	R8077	1.0
R8075	R8074	0.8



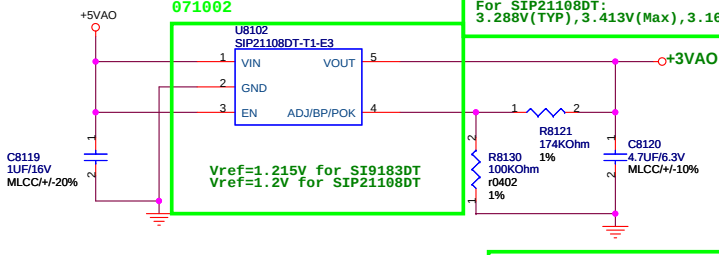
+3VA0

BOM need add second source:
SI9183 (06G007055114)

071002

For SI9183DT:
3.329V(TYP),3.473V(Max),3.178V(min)

For SIP21108DT:
3.288V(TYP),3.413V(Max),3.163V(min)



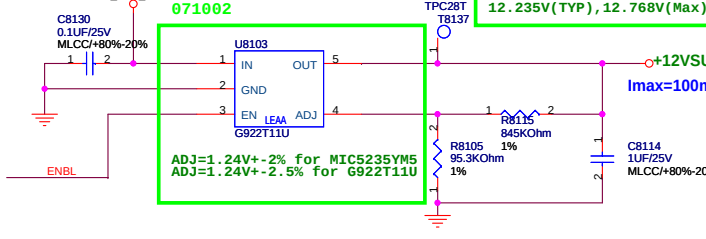
+12VSUS

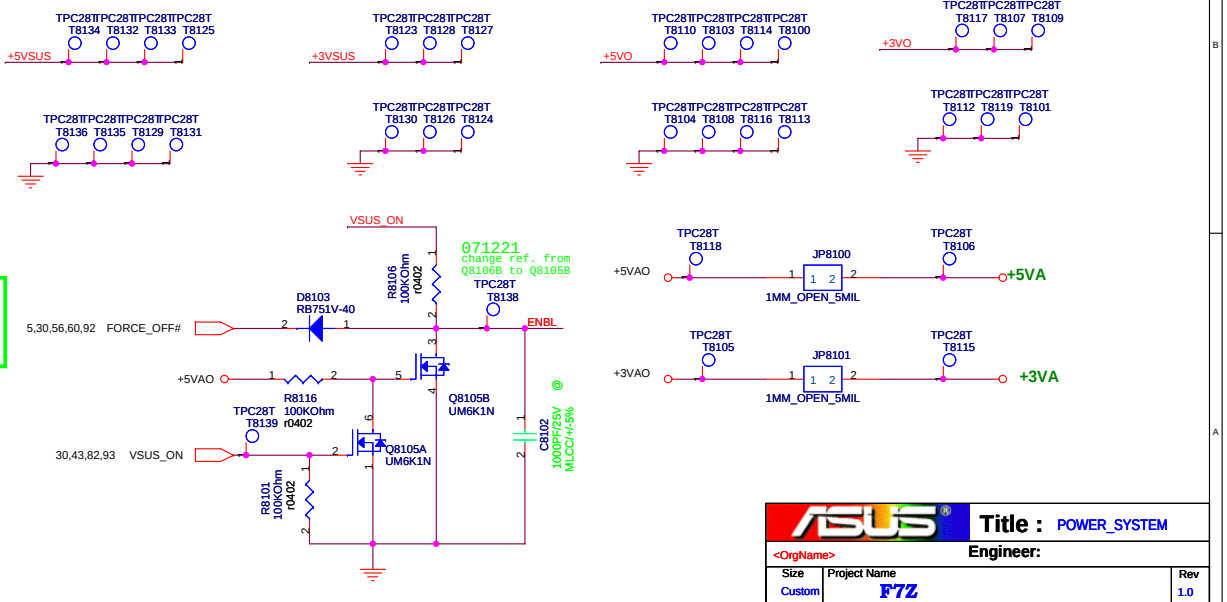
BOM need add second source:
MIC5235YM5 (06G007137020)

071002

For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)

For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)





ASUS	Title : POWER_SYSTEM		
<OrgName>	Engineer:		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 81 of 94		

* Rocset = Ioc * DRC / 10uA

+1.2VO: ROCSET = R8213 ; R8215 = R8213=10KOhm; OCP>7.5A

+1.8VO: ROCSET = R8212 ; R8212 =R8211 =4.7KOhm ; OCP>14A

* VREF = 0.6V+-1%

+1.2VO = VREF * (R8206 + R8214) / R8214 =1.2V+-2%

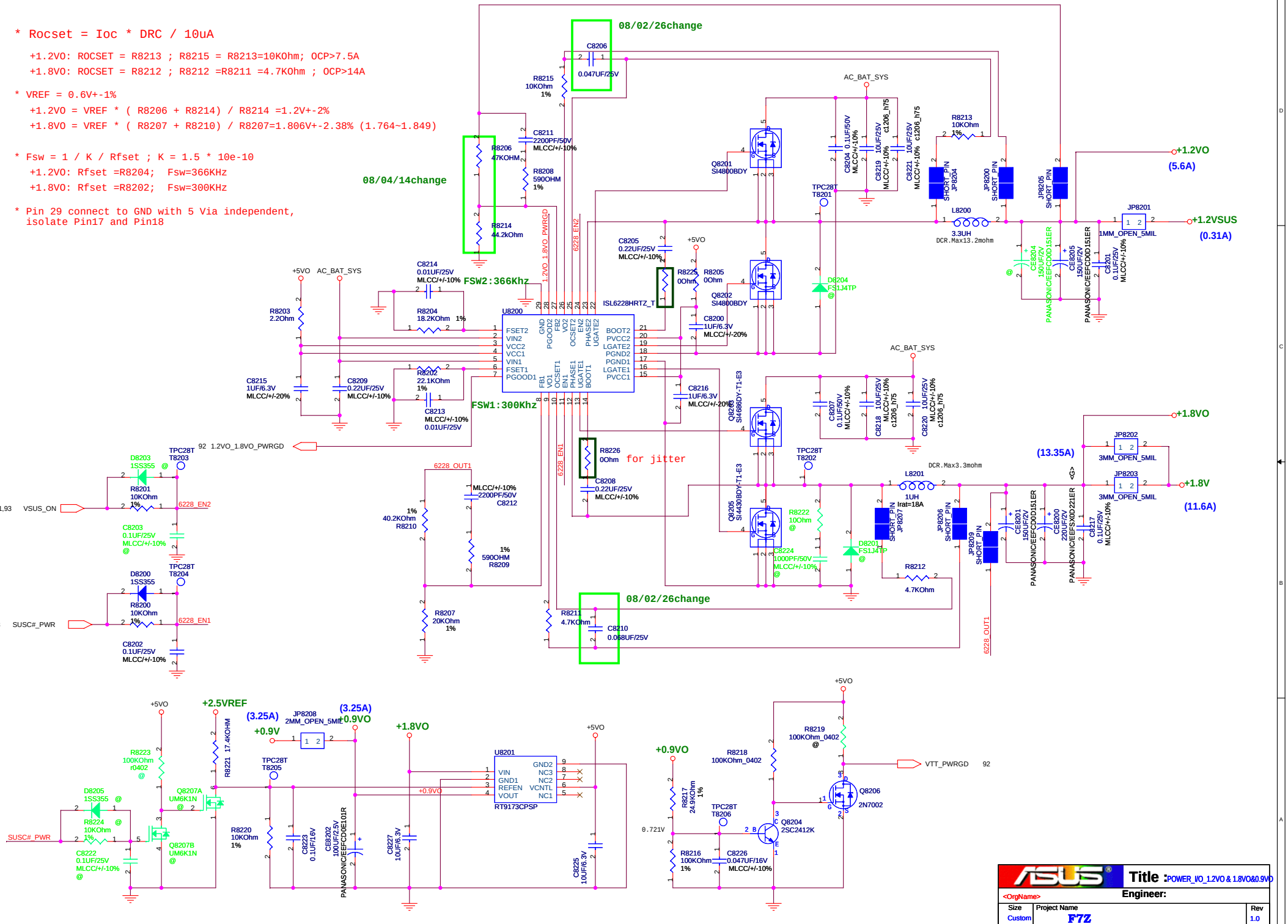
+1.8VO = VREF * (R8207 + R8210) / R8207=1.806V+-2.38% (1.764~1.849)

* Fsw = 1 / K / Rfset ; K = 1.5 * 10e-10

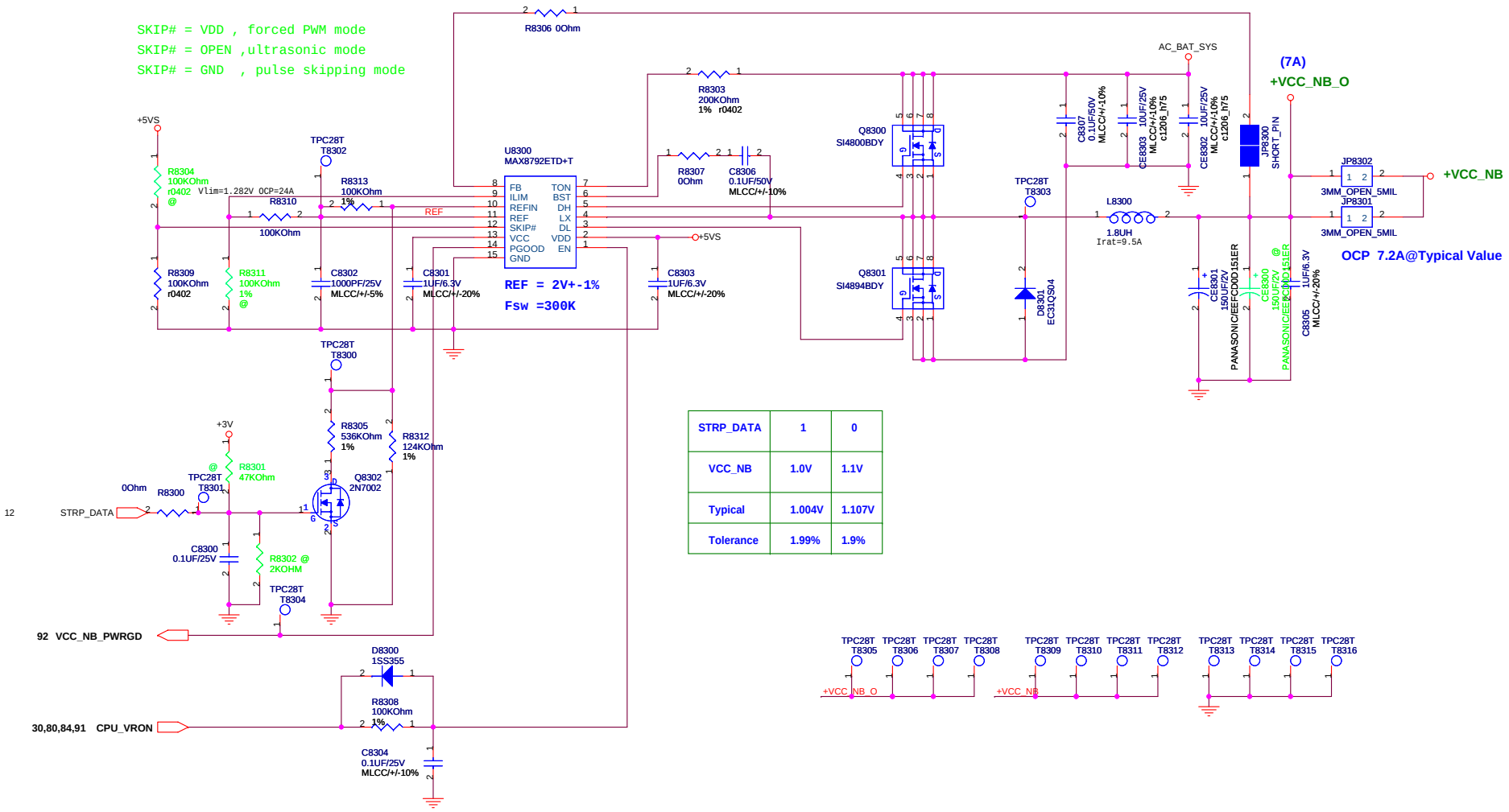
+1.2VO: Rfset =R8204; Fsw=366KHz

+1.8VO: Rfset =R8202; Fsw=300KHz

* Pin 29 connect to GND with 5 Via independent, isolate Pin17 and Pin18



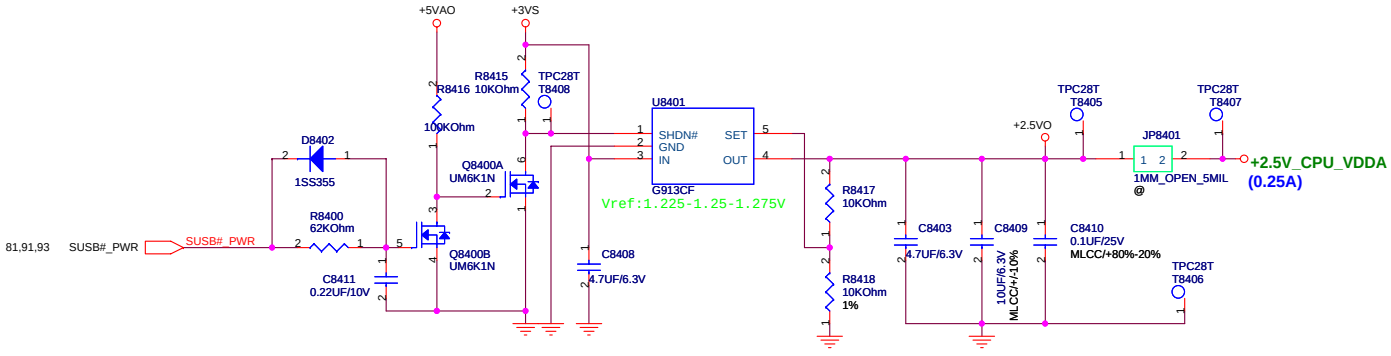
Title : POWER_I/O_1.2VO & 1.8VO&0.9VO		
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 82 of 94	



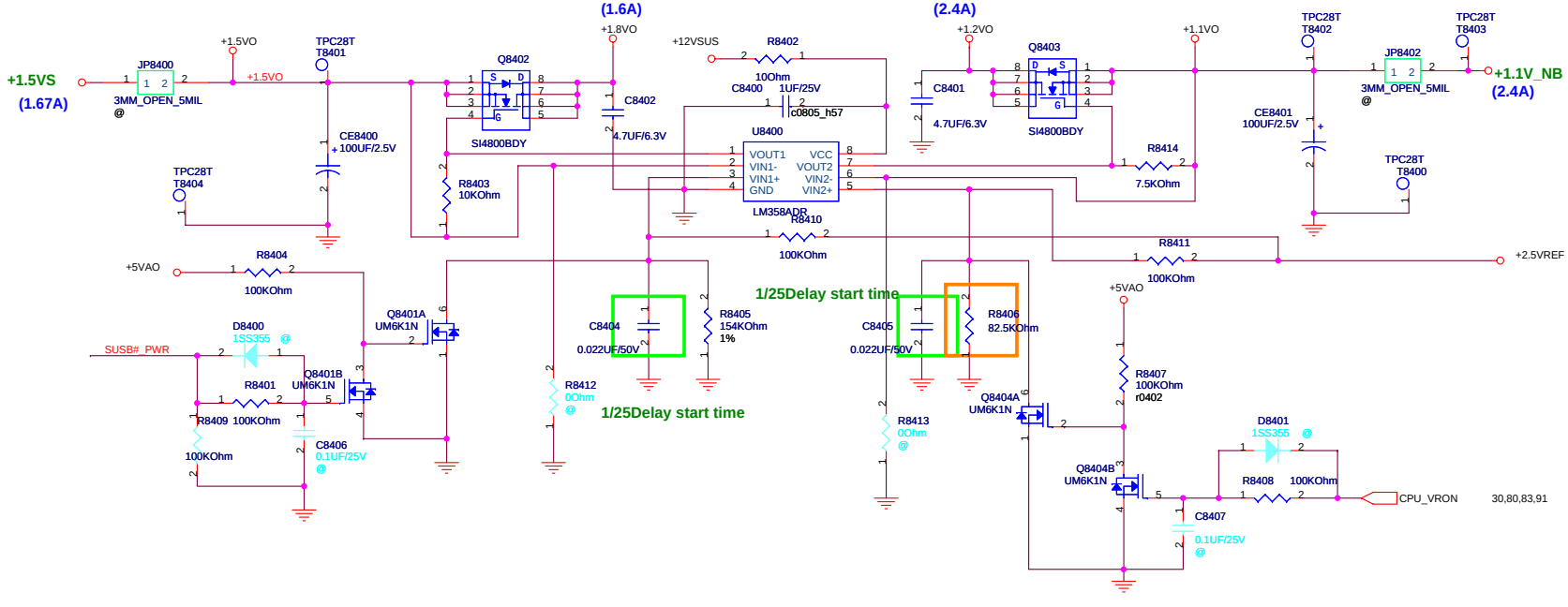
STRP_DATA	1	0
VCC_NB	1.0V	1.1V
Typical	1.004V	1.107V
Tolerance	1.99%	1.9%

Title : POWER_I/O_VCC_NB		
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 83 of 94	

+2.5V_CPU_VDDA

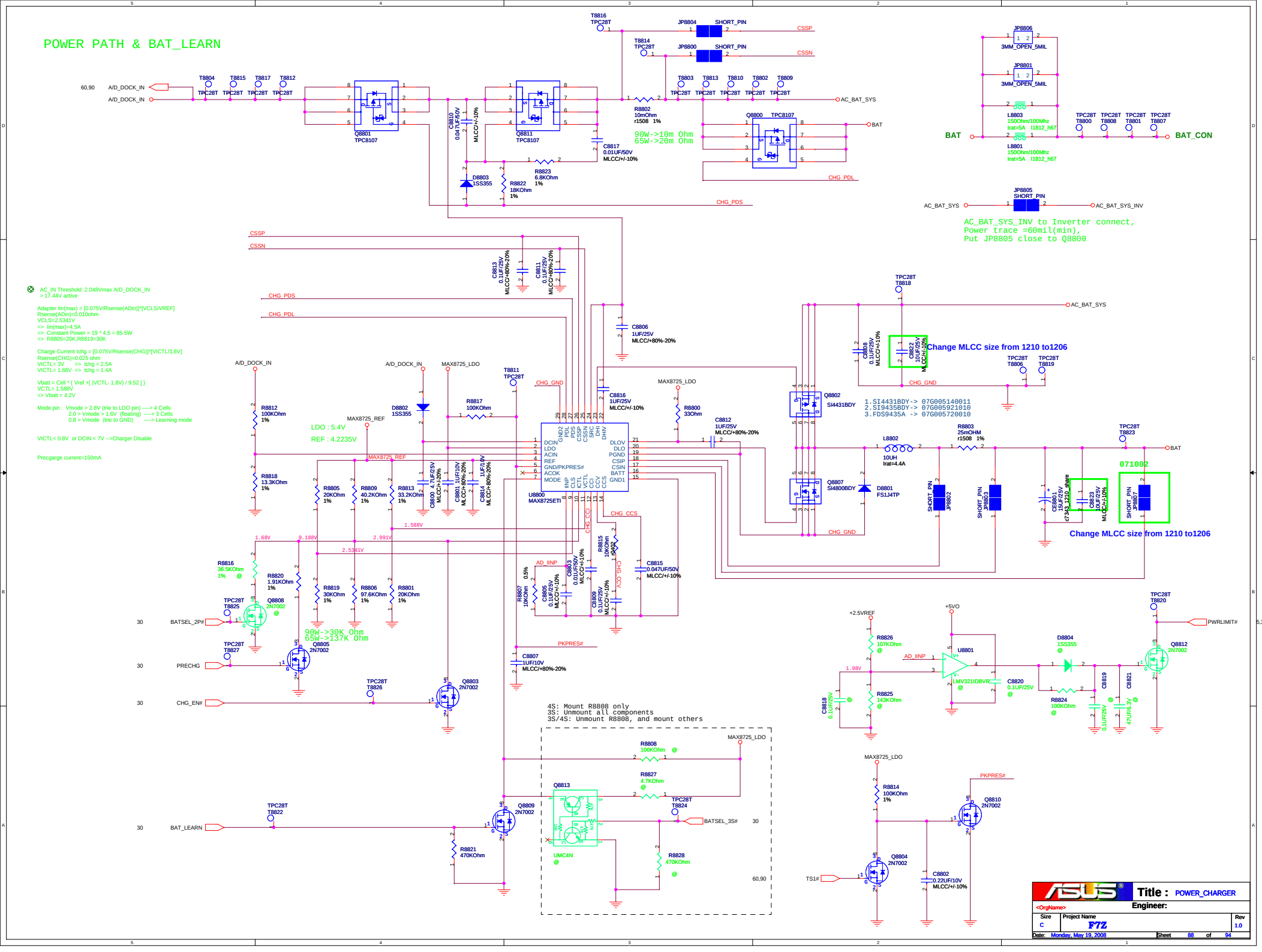


+1.5VS & +1.1V_NB

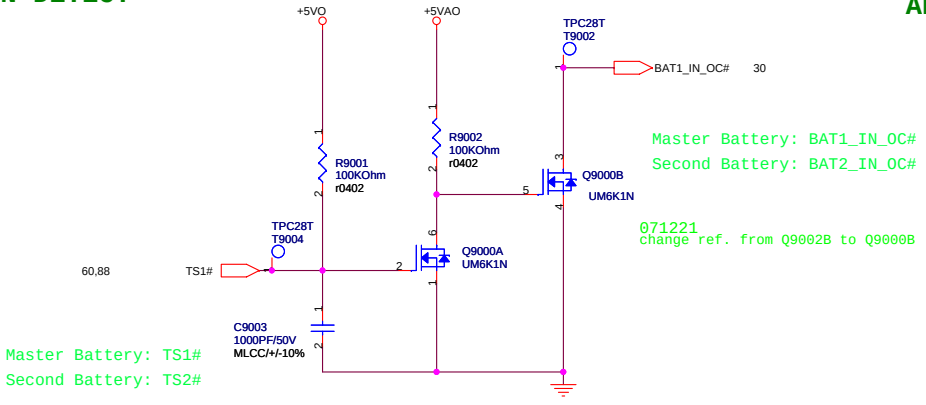


ASUS	Title : POWER_+2.5VS&+1.5VS & +1.1VS		
<OrgName>	Engineer:		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 84 of 94		

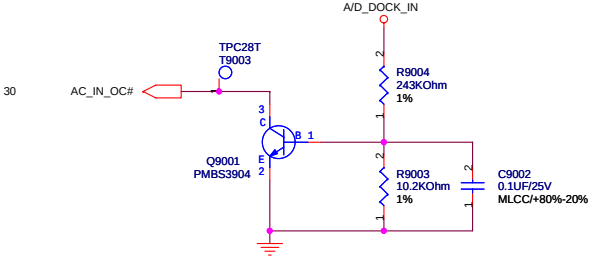
POWER PATH & BAT_LEARN



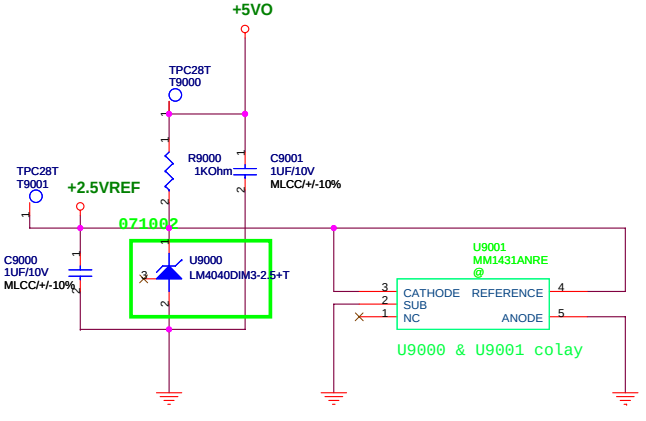
BATTERY IN DETECT



ADAPTER IN DETECT



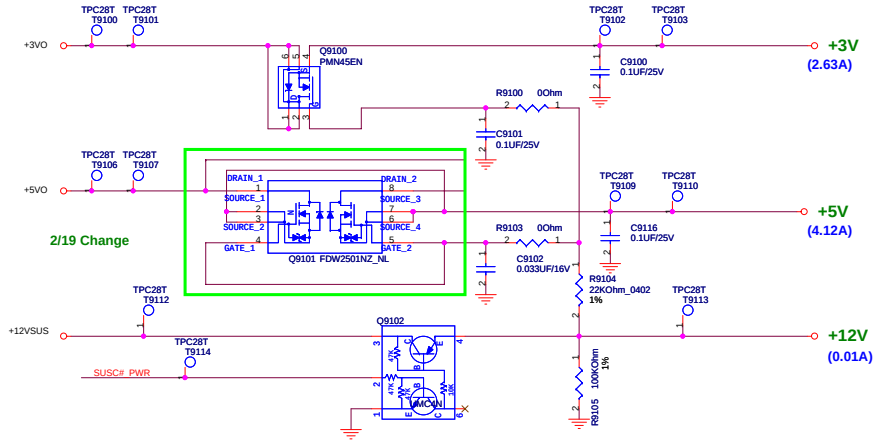
+2.5VREF

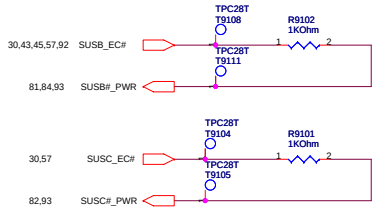


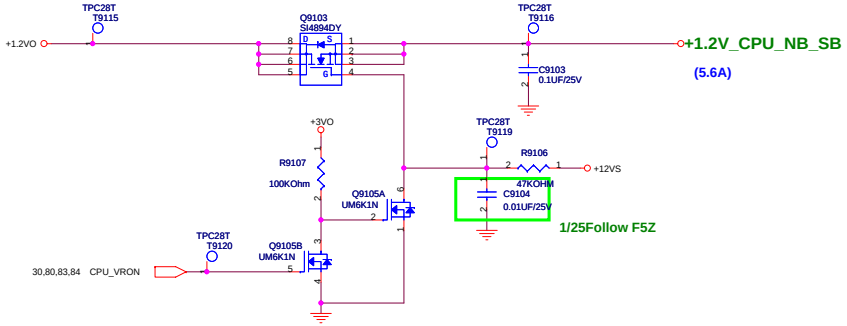
U9000 Main source change to 06G006002414(tolerence:1%).
Add second source 06G006002610 (tolerence:1%),
06G006002412 (tolerence:0.2%) and
06G006002020(tolerence:0.2%)

ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 90 of 94	

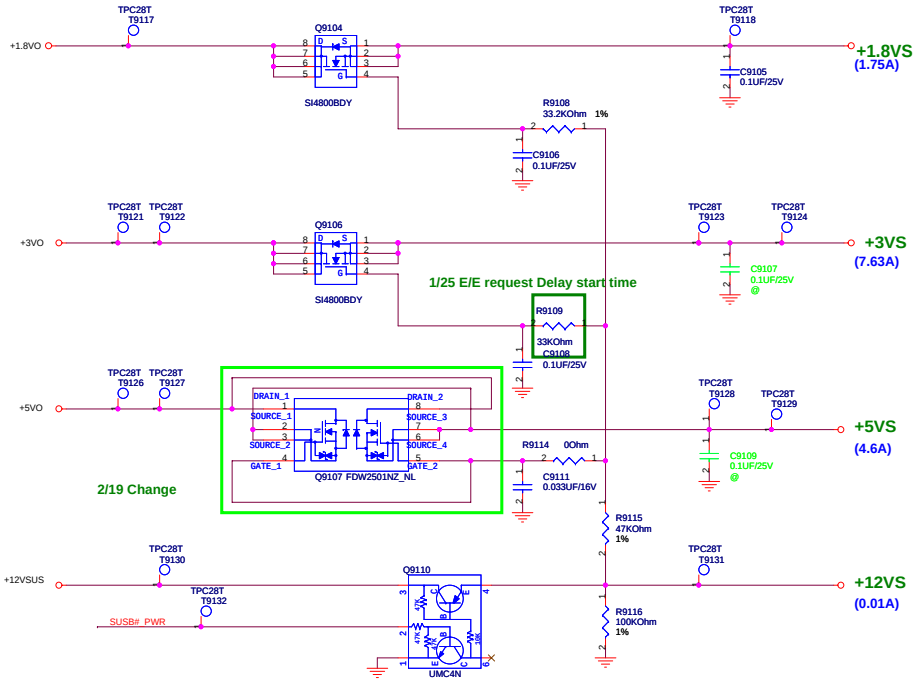
SUSC#_PWR POWER





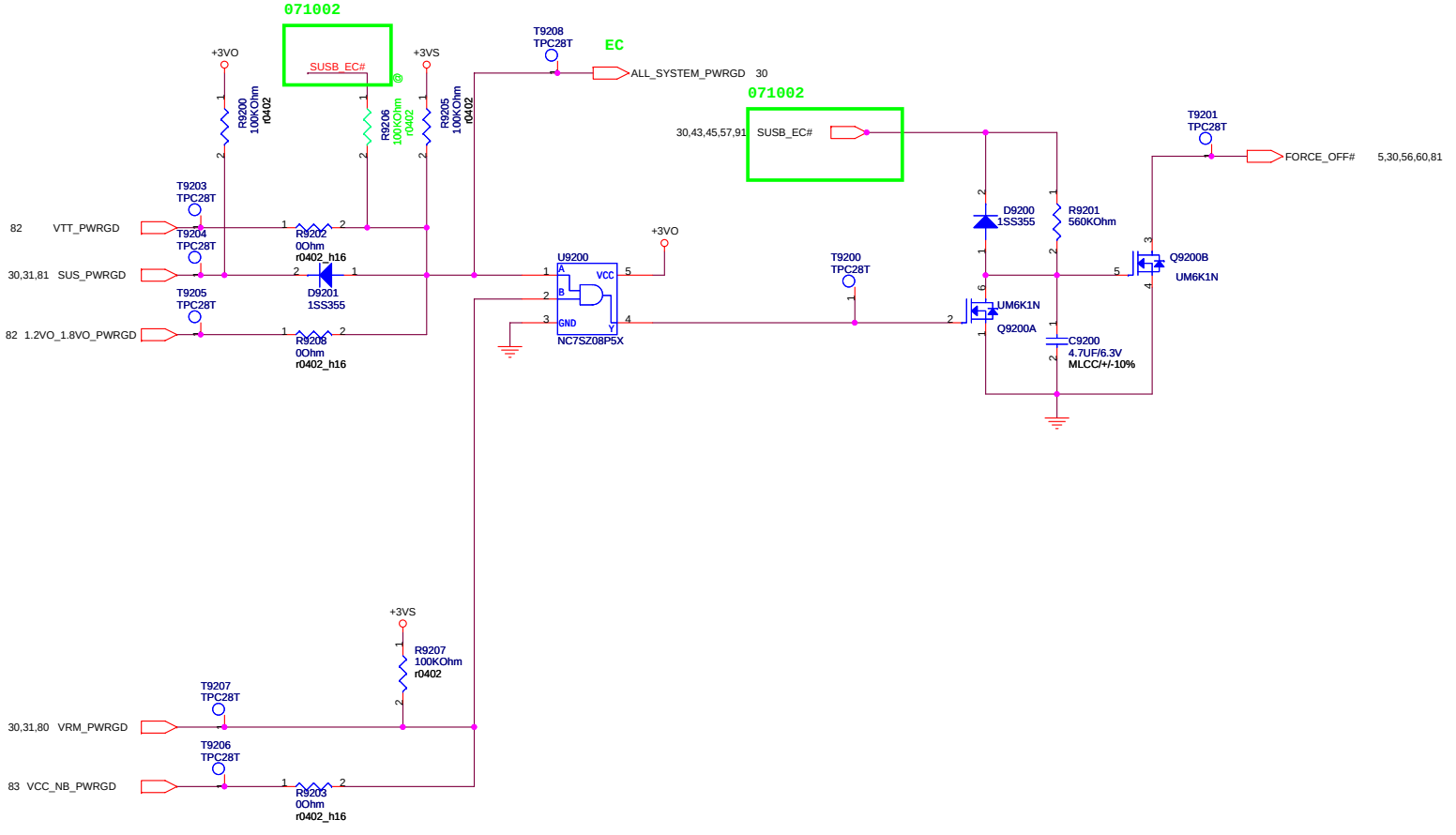


SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 91 of 94	

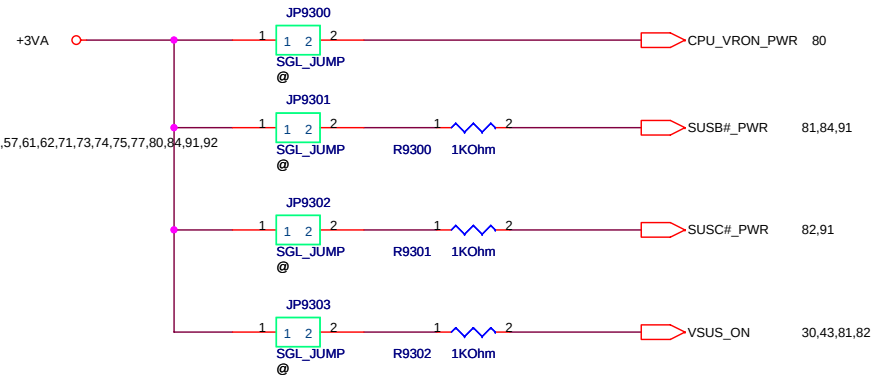
POWER GOOD DETECTER



ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 92 of 94	

AC_BAT_SYS	AC_BAT_SYS	60,80,81,82,83,88
BAT	BAT	60,88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	82,84,88,90
+3VA	+3VA	20,30,45,56,57,61,62,81
+5VAO	+5VAO	81,84,90
+5VO	+5VO	81,82,88,90,91
+5VSUS	+5VSUS	81
+5V	+5V	44,45,52,57,91
+5VS	+5VS	23,30,31,36,37,46,50,51,57,71,80,83,91
+3VO	+3VO	56,81,91,92
+3VSUS	+3VSUS	4,20,21,22,23,24,30,33,35,37,43,53,56,80,81
+3V	+3V	30,35,44,45,53,55,57,61,62,83,91
+3VS	+3VS	5,7,8,12,13,14,21,22,23,24,29,30,31,33,36,37,43,45,46,50,51,53,55,56,57,61,62,71,73,74,75,77,80,84,91,92
+12VSUS	+12VSUS	81,84,91
+12V	+12V	37,57,75,91
+12VS	+12VS	30,45,57,71,91
+1.8VO	+1.8VO	82,84,91
+1.8V	+1.8V	4,5,6,7,8,9,57,82
+1.8VS	+1.8VS	5,12,13,14,21,57,91
+0.9V	+0.9V	4,6,9,57,82
+0.9VO	+0.9VO	82
+2.5V_CPU_VDDA	+2.5V_CPU_VDDA	5,57,84
+1.5VS	+1.5VS	43,53,55,57,84
+1.5VO	+1.5VO	84
+1.1VO	+1.1VO	84
+1.1V_NB	+1.1V_NB	12,14,57,84
+1.2VO	+1.2VO	82,84,91
+1.2VSUS	+1.2VSUS	23,82
+1.2V_CPU_NB_SB	+1.2V_CPU_NB_SB	3,14,20,22,23,57,91
+VCC_NB_O	+VCC_NB_O	83
+VCC_NB	+VCC_NB	14,57,83
+CPU_VDD0	+CPU_VDD0	6,57,80
+CPU_VDD1	+CPU_VDD1	6,57,80
+CPU_VDDNB_O	+CPU_VDDNB_O	80
+CPU_VDDNB	+CPU_VDDNB	6,57,80

FOR POWER TEST



Title : POWER_SIGNAL		
<OrgName>	Engineer:	
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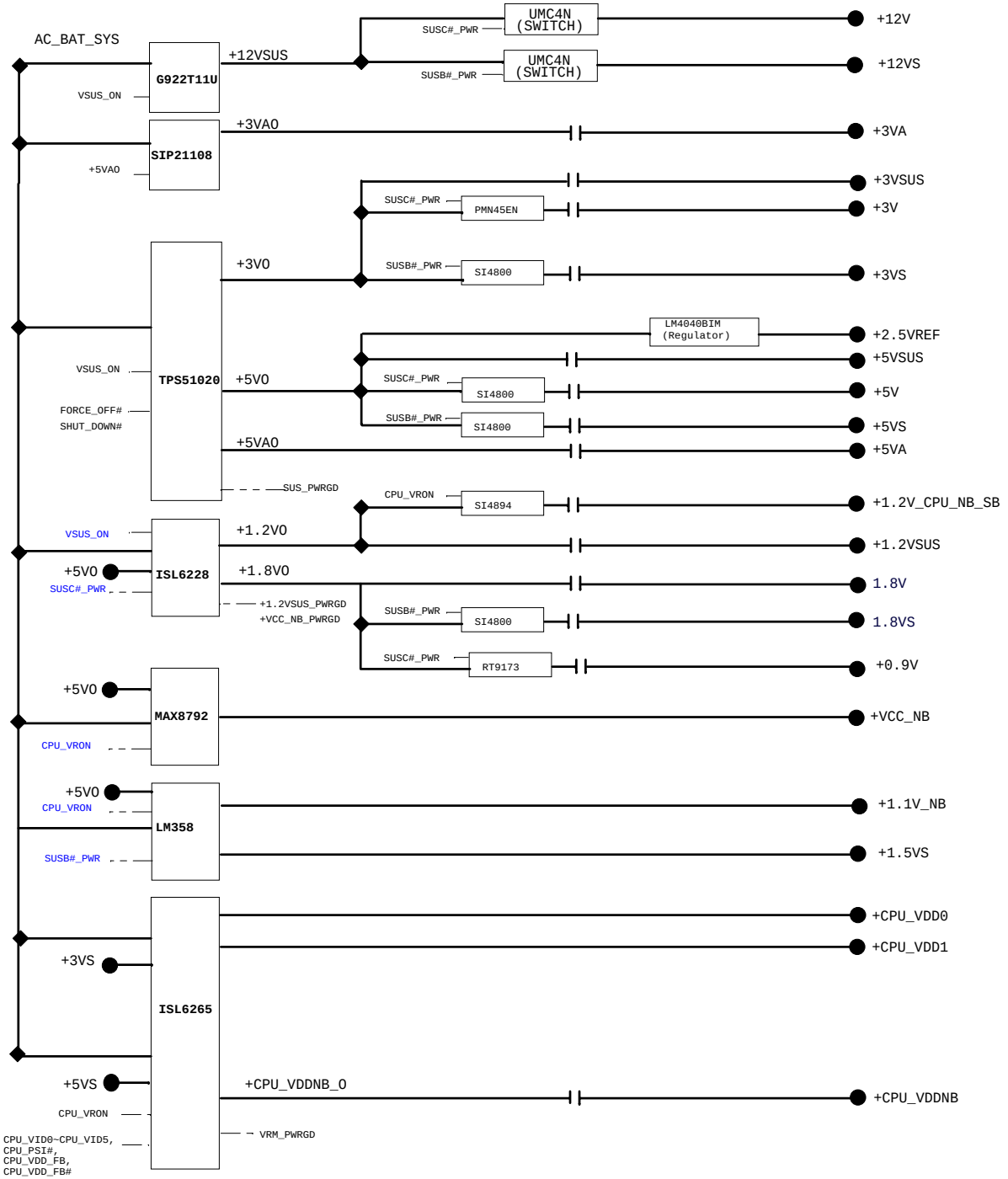

ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 94 of 94	